SEMICON, PACKAGING & ASSEMBLY REPORT
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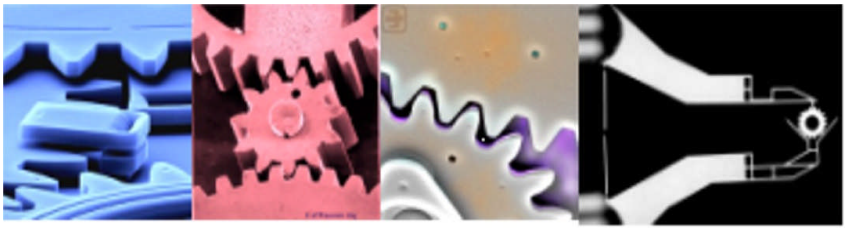
ET TRENDS

BUSINESS NEWS

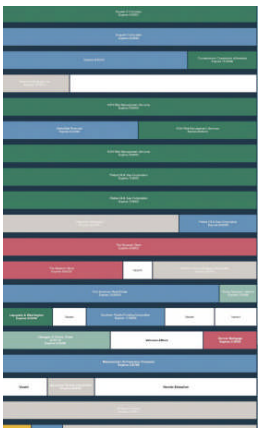
More and More Silicon - Worldwide silicon wafer area shipments (by surface area) increased by 20% in 2006 when compared to 2005 shipments according to SEMI's Silicon Manufacturers Group (SMG) in its year-end analysis of the silicon wafer industry. Revenues also grew by 27% in 2006 because of 300-mm contributing to an overall better product mix. Silicon wafer shipments in 2006 totaled 7,996 million square inches (MSI), up from the 6,645 million square inches shipped during 2005. Revenues grew to $10-billion from $7.9-billion posted in 2005. This made 2006 a very robust growth year for the silicon wafer suppliers in terms of both units and revenue. This was driven in a large part by the increased demand for memory products in both the 300-mm and leading edge 200-mm segments. The growing demand for solar will also be an increasingly important factor.

The Future of MEMS will be consumer-driven. MEMS merges perception, computation and actuation in devices that combine chemistry, telecommunications, medicine, cinema, optics, electronics and mechanics according to Gartner. "It is the convergence of science and technology. MEMS is enabling "the ultimate systems-on-a-chip." *[Gilleo quotes?]*. The current MEMS market is expected to accelerate over the next few years as consumer products begin driving the market. MEMS manufacturing technology combines both mechanical and electronics properties, and is compatible with nanotechnology. By 2010, according to Gartner, MEMS components could be a $10- billion market, while products enabled by MEMS technology could grow to as much as $95 billion. Among the most visible MEMS applications are digital light processors, which integrate millions of tiny mirrors onto a chip to enable ultra-bright projection displays. Other automotive applications like airbags have been around even longer. Automotive applications will continue to use more MEMS-based sensors like wireless tire-pressure sensors. But the fastest growing MEMS areas in the next few years will be consumer devices. Silicon microphones [plenty of lawsuits here] are already being used in cellphones and that trend will increase; also, accelerometers and gyroscopes will be added to Global Positioning Systems as well as shock detectors in laptops and in cellphones. MEMS-based biomedical sensors and implants are another potential growth market along with optical switches that could eliminate bulky, expensive optical-to-electronic-to-optical switches.



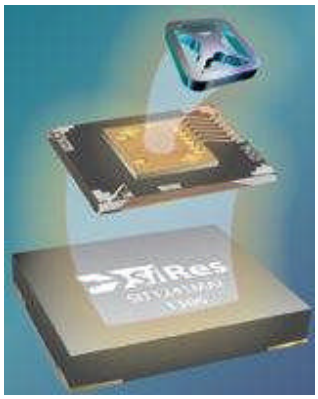
Intel's X11 - Intel will invest up to $1.5-billion to retool its Fab 11X located in Rio Rancho, N.M., for **45-nm** manufacturing, making it the company's 4th factory scheduled to use the 45-nm process set to begin in Q2-2008. The 45-nm high-k and metal gate process consists of a combination of new transistor materials aimed at reducing transistor leakage and increasing performance. Intel will use a new material with a higher-k dielectric constant, along with a new combination of metal materials for the transistor gate electrode. Early versions of its 45-nm family of products (Penryn) are already running multiple operating systems and applications and Intel says it is on schedule. The new 45-nm process represents one of the most significant manufacturing breakthroughs in decades. The Rio Rancho site has successfully operated in New Mexico for 27 years. Initial production of Intel's 45-nm products will be done at its Oregon development fab, D1D. The company is currently building two other factories that will use the 45-nm process. The $3 billion Fab 32 in Chandler, Ariz., will begin production late this year; and the $3.5 billion Fab 28 in Kiryat Gat, Israel, will begin production the first half of 2008. Fab 11X currently manufactures 90-nm computer chips on 300-mm wafers, began production in October 2002 as Intel's first 300-mm manufacturing facility, and was Intel's first fully automated, high volume factory producing 300-mm wafers.

The Stacking Business - 3D Integration for MEMS, image sensors and memory is gaining momentum. *[While the areas are different, there is synergy]*. The technical issues for innovative 3D packaging at the wafer level are close to be solved. Semiconductor chips face constant pressure for increased performances while still decreasing their size and at the same time, their packages must be able to accommodate new functionalities. The ever-expanding consumer electronics market is a particularly strong driver of packaging innovations such as 3D ICs. Today wire bonding is limited in density and performances so 3D stacking with micro-vias (or TSV, "Through-Si Vias") is unavoidable in the future for miniaturization first and increased performances after. 3D integration will use technologies originally developed for MEMS technology but for different markets. The portable applications are a strong market driver for 3D integration. Stacking memories, stacking memories + logic, image sensors with µP and FPGAs will be the first mass market applications. In 2010, the forecast that 1 billion of Flash memories will be stacked using TSVs according to Yole. 3D is the most "integrated" approach and is an enabling technology platform applicable to digital and mixed signal electronics, wireless, electro-optical, MEMS, sensors, smart imagers, displays and other devices. There are however strong challenges: thermal management; reliable co-design and simulation tools, industrial wafer-to-wafer bonding tools, low-cost through-wafer via structures and via fill processes. *[Recent IP search shows that via drilling and filling (mostly Cu plating), are areas of focus with circuit design and wafer interconnect/bonding also starting to show up. OPPORTUNITIES]*.



MEMS & BIO-CHIPS

Oscillators - SiTimes announced MEMS oscillator design wins from 3 unidentified customers, including one order for 1 million units. All 3of the companies make consumer electronics devices, including cellphones. The oscillators will allow the customers to shrink their devices by eliminating bulky quartz crystals from their pc-boards. When SiTime adds quartz crystal makers like Micro Crystal (Grenchen, Switzerland) to its customer list, it will boast orders for over 50 million MEMS oscillators. They are also receiving significant orders for our standalone MEMS resonator. These orders are coming from customers who already have a phase- locked loop working in their design, and just want to eliminate the quartz crystal from their circuit board. SiTime's oscillators consist of two chips, one for the MEMS resonator and a second stacked die for an ASIC holding the PLL and its signal conditioning circuitry. Besides standard stacked-die parts, SiTime now claims to have orders from three major semiconductor makers for custom resonators that will be stacked onto ASICs *[emerging packaging opportunity?]*. SiTime also announced an integrated oscillator chip that includes a MEMS resonator on the bottom layer of the die and ASIC circuitry fabricated on the top of the same chip. Cost wise, it is still cheaper to bond the MEMS die together with the ASIC, but for some applications, it does make sense to integrate both onto the same die.



TECHNOLOGY FOREFRONT

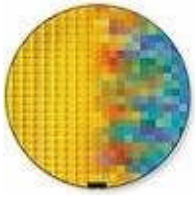
Phase-Change Memory for 2007 - Intel is preparing to sample a 128-Mbit phase change memory to customers in the first half of 2007. Mass production could begin before the end of 2007. The memory is being introduced as a drop-in replacement for NOR flash non-volatile memory although its performance characteristics means it could be used it a greater range of applications and come to replace in DRAM in some systems. Intel has been a licensee of chalcogenide-based phase change memory technology from **Ovonyx**, a wholly-owned subsidiary of Energy Conversion Devices Inc. (Rochester Hills, MI) since 2000. Over this period, Intel has been actively researching the technology even though Energy Conversion Devices has been touting the technology, without commercial success, for more than 30 years. Intel and European chipmaker **STMicroelectronics** also announced they had teamed up their research on chalcogenide-based phase-change memory as a likely successor to flash as a non-volatile memory, in June 2006. Interest in phase-change and other non-volatile memory technologies has increased markedly in the last five or six years as there are increasing concerns that flash memory may struggle to scale. **Qimonda** (formerly the memory operation of Infineon) is researching phase-change memory technology with **IBM** Corp. and **Macronix**, **Renesas** and **Hitachi**, also disclosed a phase-change non-volatile memory module for integration on microcontrollers used in embedded systems. Intel's

128-Mbit phase-change memory had demonstrated 100 million read-write cycles of endurance and a capability for much greater than 10 years data retention. The phase-change memory gets pretty close to perfect and will start to displace some of the RAM in the system.

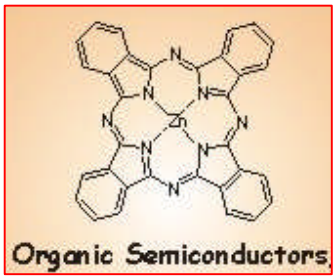
Deep Silicon Etching for 3-D Integration - Through-silicon via (**TSV**) etching is used to manufacture MEMS, power devices and, lately, ***3-D stacked chips***. Device manufacturers and packaging houses are looking to wafer-level packaging (WLP) techniques to address the demands of future product miniaturization and increased functionality. Products that will ultimately benefit from this type of scaling include digital cameras, cell phones and PDAs. 3-D integration is one type of WLP method whereby two or more planar devices are stacked and connected. Multiple approaches in WLP include wire and flip-chip bonding, but a more sophisticated and performance-enhancing method involves the use of through-wafer vias. In 2007, the International Technology Roadmap for Semiconductors (ITRS) will incorporate and track the design nodes and architectures for 3-D interconnect for the first time. *[Most of the memory producers are developing TSV processes for stacked memory and there are already thousands of patents and applications - KG].*

Deep silicon etching, based on the Bosch process, was originally conceived and is still being used for MEMS device fabrication. However, it is also an enabling technology for new ranges of power devices (deeper trenches for higher voltage and current handling) and etching through-silicon vias. The process involves fast switching between silicon etching and polymer deposition for silicon sidewall protection, with SF6 and C4F8 being the principal process gases for the etch and deposition cycles, respectively. Benefits of the switched approach (typical step times being 1-3 sec) include high etch rates and mask selectivities that cannot be achieved by single-step silicon etching. A disadvantage is “scalloping” of the sidewall, an artifact of the etch and deposition cycles. However, with proper process optimization, scalloping can be minimized. Deep silicon etching is an enabling technology for 3-D packaging. Successful integration of through-silicon vias will require close cooperation between etch, oxide deposition and metal seed/fill providers. Cost models for these new technologies are still being calculated, and the logistics of how to “fit” the technology into the existing IC food chain will continue to be explored and discussed. *[This is an area to track].*

The 80-Core Tera - Intel has developed a programmable processor that delivers supercomputer-like performance from a single, 80-core chip. This "Tera-scale computing" processor is aimed at delivering Teraflops (trillions of calculations per second) for future PCs and servers. Intel India Development Center (IIDC) played a central role in the development of the Teraflops Research Chip, contributing about 50% of the work for the logic, circuit and physical design. IIDC's Teraflops Research Chip team is part of Intel Corporate Technology Group's Circuit Research Labs established in June 2004 with a center in Oregon and another in India. Intel-India has

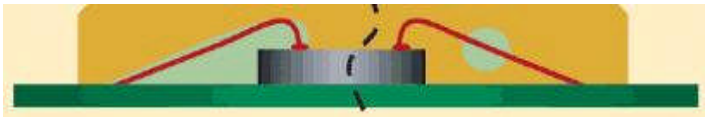


demonstrated immense talent and potential and advanced into the "era of tera" *[and corny phrases]*. Intel has no plans to bring this exact chip designed with floating point cores to market. However, the company's Tera-scale research is instrumental in investigating new innovations in individual or specialized processor or core functions, the types of chip-to-chip and chip-to-computer interconnects required to best move data and, most importantly, how software will need to be designed to best leverage multiple processor cores. This Teraflops research chip offered specific insights in new silicon design methodologies, high-bandwidth interconnects and energy management approaches.



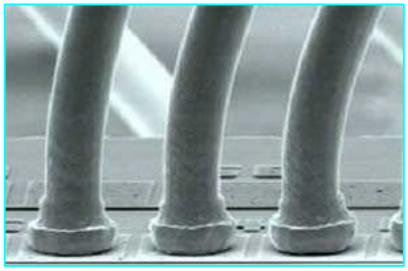
Organic Semiconductors - There's considerable work going on in the organic semiconductor field. Korean researchers have made a flash-like non-volatile memory cell using polymers. The experimental device is partially traditional inorganic silicon technology: a conductive silicon substrate covered by a 300mm SiO2 oxide layer. The substrate acts as a gate and the oxide as a gate insulator. Above this is a polymeric gate dielectric layer (poly-methylstyrene; PaMS) and a semiconducting pentacene layer with source and drain contacts. Without the PaMS layer, the device has FET-like characteristics with a stable gate threshold voltage. With the PaMS layer, it also behaves as a FET, but the threshold voltage can be reversible altered by applying high positive or negative biases to the gate. This is similar to a flash cell where the gate of a silicon FET not only operates the device's channel, but at higher voltages injects electrons into a separate "floating" gate altering the cell's threshold voltage -- allowing it to store a bit of data. But data retention is 100 hours - not long enough for practical data storage.

MATERIALS



Wire Drop Encapsulation for Fine-Pitch Revisited - K&S reported work on a modified wire encapsulation process for very fine pitch packaging a while ago, but it may merit another look. Modern leading-edge wire bonders are capable of 35-µ inline pad pitch in production environments. They have been able to overcome wire count limitations by developing multi-tier staggered pad bonding over active circuitry. Wire cycle speeds are up to more than 16 wires per second; translates into production throughput rates of 10-13 wires per second. In addition, wire bonders have proved to be most effective in bonding stacked die in 3-D packages. Wire sweep occurs when bonded wires are not correctly aligned in the horizontal plane (as opposed to wire sag, which is in the vertical orientation). Wire sweep can occur during the wire bonding process, handling after wire bonding, or during molding. Wire sweep is undesirable, as it can affect electrical performance by changing the mutual inductance of adjacent wires and simultaneous switching noise. If the wires actually touch, they will short. Polymer encapsulation can help. Conventional encapsulation materials and processes are not adequate for sub-35 µm spaced wires. Corner gate molding was not successful on 35 µm pitch die with 15 µm wire diameter

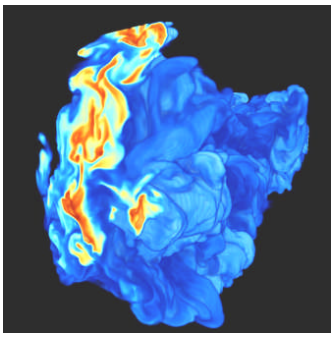
and 4.7 mm long gold wires. The molding materials and parameters simply moved the wires too much because of the flow characteristics of the materials. The problem is that standard molding compounds are primarily comprised of spherical silica filler. Typically, this filler has an average diameter distribution that can be higher than the gaps between the fine-pitch wires. Trying to inject this material through the wires causes wire movement.



The move below 45-µm pad pitch has generated a new set of challenges that are stretching the capabilities of conventional processes and materials. Many new mold compounds with lower viscosity and smaller filler diameter are being developed for use in conventional edge gate and new center gate molding processes, but there are significant technical challenges. The materials use smaller average particle size fillers, which increase the compound's viscosity. The increased viscosity generates more drag on the wires during injection. Therefore, the higher surface area of the smaller fillers must be offset by lower viscosity resins and slower injection speeds. Tests with several of these new encapsulation materials at K&S have demonstrated 10% reduced sweep in an edge gate molding process to 30% reduction using low-sweep mold compounds. Approximately 5% overall sweep was achieved for corner gate molding at 35 µm with low flow compound in a collaborative test with plastics pioneer, Sumitomo Bakelite. Researchers expect yield loss caused by sweep to be further reduced by lowering productivity or raising material costs. Additionally, many of these developmental compounds have not yet passed JEDEC 2A, 260°C reflow reliability testing at OEMs.

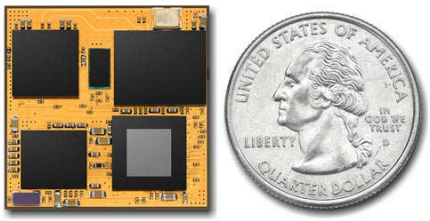
Wire insulation technology (new/old idea) could help. Insulated wires could alter the way companies approach device design and process engineering. Devices could become far more complex if wire touching were no longer a concern. This capability would be a boon to the rapidly expanding stacked-die packaging market, enabling almost unlimited design flexibility. And the focus of wire bond process engineers would shift rapidly from loop profiles to bond integrity. At least two wire manufacturers offering wire with an insulated coating. This technology, used for a century in magnet wire, has been in stop-and-go development for over 20 years for wire bonding applications. But the coating can create removal and bonding issues. But a new patented, sweep-resistant encapsulant technology offers a unique solution to sweep. This silica-filled liquid polymer (Polysciences) easily disperses to encapsulate wires, locking them in place and prohibiting their movement during process transition and transfer molding. The material is dispensed onto the wires immediately after wire bonding, flowing easily between and around the wires without causing sweep, sag (wire in the Z direction) or voids. Quickly jelled with UV, wires are secured in place so that the device can be handled and molded without damage. Test results at assembler locations show that sweep decreased from 6.5% using conventional molding process and material to only 0.12% using the sweep-resistant encapsulant technology. *[This is actually a 2004 paper but is this an area for new materials and equipment - Fluid Jetting? as 3D stacking gains?]*

Time Has Come for Jetting? - MacDermid and New System introduced CircuitJet, an Ink Jet Innerlayer Etch Resist Technology. This is an ink jet primary image etch resist for innerlayer manufacture. In partnership with New System, SrL, the technology combines the latest in innovative ink jet equipment design with a high resolution UV-curable etch resist ink. CircuitJet™ is a unique, patent-pending process that delivers the capability to produce the highest technology innerlayer circuit patterns with direct ink jet printing. This process produces layers "ready for etch" with reduced cycle time, while eliminating the need for all artwork, photo tools, lamination, exposure and developing.

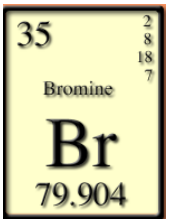


PCBs PACKAGING & ASSEMBLY

Freescale announced that it is setting up a pilot production line at its facility in Tempe, AZ for its redistributed chip packaging (RCP) technology in preparation for volume manufacturing. Freescale its RCP technology, first announced in July 2006, could replace BGA and flip chip as the dominant packaging and assembly approach for advanced semiconductors by consolidating electronic components into a single miniaturized system. RCP integrates semiconductor packaging as a functional part of the die and system solution, and purportedly eliminates wire bonds, package substrates and flip chip bumps. In addition, RCP does not utilize blind vias or require thinned die to achieve thin profiles. The new technology recently passed several commercial technical specifications for reliability and durability including Moisture Sensitivity Level 3 with 260 degrees C reflow testing; 1500 cycles of air-to-air thermal cycling after pre-conditioning; and 96 hours of unbiased Highly Accelerated Stress Test (HAST) after pre-conditioning. The company has said it expects products utilizing RCP technology will be available by 2008.



Halogen-Free Intel - Intel has stopped using halogens in the packaging for its Flash memory for mobile phones. The chip firm's use of halogens in molding compounds, solder masks and the core substrate meant these products couldn't be recycled. Halogens are highly reactive substances that can cause damage to the ecosystem. It's not clear which halogens have been present in Intel's Flash packaging up until now. The firm said it had made the change following requests from its customers.



China JV - NXP Semiconductors and ASE (Advanced Semiconductor Engineering) have signed a memorandum of understanding to form a joint venture (JV) in Suzhou, China, focused on semiconductor testing and packaging. NXP (formerly Philips Semiconductors) will hold a 40% share while chip testing and packaging specialist ASE will hold the remaining 60%. The JV will serve the international and domestic Chinese markets and will be located at

NXP's existing manufacturing site in Suzhou, noting that the JV is expected to begin operations in Q2-2007. NXP said it will contribute its existing testing and packaging operation in Suzhou as its initial investment and noted that this agreement does not affect the other testing and packaging sites for NXP in Asia and Europe. Last month, NXP announced plans to strengthen its cooperation with foundry giant TSMC in the area of advanced CMOS development.

New China PCB Factory - Somacis PCB Industries announced the completion of the construction of its new production plant located in Chashan, Dongguan City, in the Guangdong region of China. Construction took 12 months for the plant with a covered area of 23,500 sq.m, in a total area of 66,000 in the heart of the Chinese manufacturing industry. An annual capacity forecast at 400,000 square meters, with a workforce of 700. Investment of $33-million. Machinery and production lines are currently being installed. Production, starting in April 2007, will be specialized in high tech printed circuit boards including multilayers up to 30-layers, and HDI boards using laser-drilling technology.

PoP Continues - Toshiba announced availability of high-capacity memory system using

Package-on-Package (PoP) technology -multi-chip packaging technique by stacking a high-density memory component on top of the processor so the two components require only one footprint on the board. The initial PoP offering developed includes 14mm x 14mm and 15mm x 15mm packages fully compliant with the JEDEC standard. In a cellular handset PoP configuration, two Ball Grid Array (BGA) packages are stacked vertically. The bottom package, typically an applications processor, has the usual array of metallic balls, or bumps, on the underside. In addition, it also has an array of footprints (lands) on the upper surface that are designed to match a compatible BGA package, typically a multi-chip memory BGA, which is soldered on top. Standardized layouts for the BGAs enable signals to be routed between the two components. [PoP can be traced back to the 70's, so this is more business as usual than a breakthrough. But expect to see PoP and Chip2Chip packages proliferate as part of the present package revolution]

New PCB Process from Korea? - Engineers claim to have developed an eco-friendly method of producing printed circuit boards (PCBs) that are an integral part of all electronic appliances, the Korea Institute of Industrial Technology. They devised a new manufacturing system that produces multi-layer, flexible, printed circuit boards by borrowing techniques used by inkjet printers. It said the method "sprays" copper pathways onto a non-conductive substrate, forming the basis of a PCB. PCBs are the thin plates on which memory chips, central processing units, and other electronic components are placed. These components are linked by copper pathways that are created when most of a blank copper plate originally fused onto the substrate is etched away through a liquid rinsing procedure. The finished products that leave only very thin copper traces over a non-conductive substrate are cheap and reliable. However, they cause environmental pollution because liquid copper waste is produced. *[Hold it! This is just a rediscovery of Polymer Thick Film and a revisit with ink jetting of conductors].*