Wafer-Level Flip Chip: Bumps, Flux and *Underflip*

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Introduction

What's really new in modern packaging? Both Flip Chip (FC) and Chip Scale Package (CSP) have been around since the early 1960's. The ever-enduring *Packaging Revolution*, the transition from perimeter connections to area array, is trendy but we must note that the first BGA (Ball Grid Array) was actually invented in 1961 at IBM and the PGA (Pin Grid Array) has been a standard package for a long time. The PGA is easily reworkable, in fact, consumer replaceable recalling the days when upgrading was a "plug in" transaction.

The last real breakthrough in electronics was probably the integrated circuit (IC), co-invented exactly 40 years ago by Jack Kilby who had worked on printed circuits earlier [1]. The next hardware breakthrough for our all-pervasive electronics *knowledge and entertainment machines* will probably come when the electrons are swapped out for photons, but that may be a few decades away. Copper I/C metallization is really an evolution. The printed circuit community started using copper in 1903, by the way.

While not many Nobel-prize level achievements have been occurring in the packaging field, a lot of neat and clever technology is still being cranked out at a swift pace. Micropackaging is now one of the more exciting and innovative arenas for hardware technology. The two hottest packages, Flip Chip and CSP, close kin with key differences, are worth watching. The Chip Scale Package portends to be the bridge between ultimate, yet impeded Flip Chip, but the CSP adds cost with performance penalties. CSP is moving to wafer-level, but so is FC. The continuing and bothersome underfill bottleneck keeps FC from being all that it can be. Will the Flip Chip ever be fully enabled? Is CSP the real answer?

A Quick Look Back on DCA

At the beginning of solid state electronic packaging, there were only two primary chip-level interconnects – wires and joints. Now, more than three decades later, there are still only two; wires & joints. TAB (Tape Automated Bonding), a beam lead interconnect system, is still wire albeit chemically crafted wire. IBM was the first to commercialize chip-level **joint** connections with SLT (Solid Logic Technology), a transistor package using solid copper balls (the first BGA) to fabricate the first high volume Flip Chip. This was even before the famous C4 product with solder bumps. IBM's Paul Totta, *Emeritus Fellow*, points out that the Flip Chip work really began about 40 years ago (1961). The ancient but remarkably modern SLT is shown in Figure 1.

[Figure 1 – SLT courtesy of IBM]

During the 1960's, IBM, Delco and others launched Flip Chip into high volume, highly successful production. But the FC was only implemented on ceramic substrates. Back then, ceramics were the premiere high density, high reliability printed circuits. These ceramics provided the high density for mainframes, the durability and robustness for under-hood automotive but also the *close-enough* thermomechanical match for low strain Flip Chip assembly.

Going Organic – Will it Kill Flip Chip?

Most recently, Flip Chip has experienced a rebirth with the help of a technology transition. Motorola and other vertically integrated electronics companies began to move Flip Chip into the consumer product area where lower cost substrate was required. Manufacturers in Japan were also using FCs into consumer products such as their very high volume electronic watch business - still the largest use. Numerous technical problems were ultimately solved, but the solution to achieve reliability on organic PCBs was underfilling - an "alien" process. *Underfill was the solution yesterday, but it's the problem today*.

Underfill 1,2,3 or is it 8,9,10?

We foretold of the promises held by Flip Chip with its exquisite simplicity in earlier articles like "Flip or Flop?" [2] and "Flip Chip 1,2,3" [3]. Many of us then thought that the key to dazzling success was the emerging class of *snap flow snap cure* underfills [4]. Better capillary flow underfills would break the *bottleneck* so enthusiastically spotlighted by the CSP leaders. But did the "snappy" underfills break bottlenecks and set records? As it turns out, the fast flowing 5-minute cure state-of-the-art capillary flow underfills still aren't quick enough to wring out cost and aggravation for many products. What's worse, the materials have reached a performance plateau and may be close to the ***laws-of-science*** barriers. Yes, the capillary flow products work and they're in production throughout the world, but industry demands real productivity, much more productivity.

Our Flip Chip Love Affair

Our Flip Chip affair is a love-hate relationship. The love part is simple. The FC is all we could want in a package – ALMOST. There are two significant problems depending on where you are coming from. Die shrink, the size reduction of the IC geometry, is frequently used to increase performance and productivity (more chips per wafer) while cutting cost. The die shrink downside is that the chip gets outwardly smaller and that's good in most situations. But if the chip pad footprint changes, this is trouble for Flip Chip. While wire bonders only need re-program, FC assemblers may need a new circuit board. The CSP community may also need to re-fabricate their packages, but that's easier than modifying an entire multilayer PCB. There may not be an easy solution here. Bumps can be rerouted or the initial bump pattern can be pre-shrunk so that the same layout works for

the 1st and maybe the 2nd shrink. Sooner or later the FC doesn't fit the circuit PCB pads.

Yet, there is a more critical problem affecting most FCs – UNDERFILL! Not the material, but the process. Polymerized underfill works reasonably well and adds only a miniscule amount of material cost. But the common capillary flow-underfilling step wreaks havoc with the SMT methodology. Flip Chip starts off as a clean and simple SMT process with the assembly solder built right into the chip for eutectic bumped chips. The self-alignment performance of FC is extraordinary as has been shown in videos. But just when the process should be complete, another non-standard step is starting – underfilling. It's not the fill - it's the filling that hurts!

Underfilling can be the *epitome of exasperation*. It's more than a nuisance, it adds a significant amount of cost when we rigorously analyze productivity. Even a few seconds of added cycle time will translate into a large sum of money at the end of the day - a fortune at the end of the year. The cycle time increase will typically add more cost than the small savings that "no package" can offset. Once again, the underfill material cost is not the core problem – it's rather insignificant. But the underfilling step can increase manufacturing time by 50%, double floor space requirements and add significant dollars in capital equipment. We have estimated that reduced productivity from underfilling may add an extra 1-2 billion dollars per year in reduced output.

Backtracking

Did we perhaps move too quickly with organic platform 2nd generation Flip Chip and overlook something? Let's step back and examine earlier work on both flux and underfill to search for answers. In the early 1990's, flux chemists were seeking better solutions for "no clean" materials. Recall that the Montreal Protocol had banned many flux cleaners. Some of the strategies like volatile fluxes had caused significant equipment problems. Ovens were degrading and chemicals were going up the stack. Innovation was needed.

In the early 1990's, Alpha Metals "drafted" a polymer chemist to work on flux. Having no flux background but lots of polymer savvy, he hit on an unconventional approach, as is often the case. Just leave the flux in place and let it generate "nice" polymer properties during reflow. Expertise in the epoxy field led or chemist to use familiar resins as the flux carrier while choosing flux agents compatible with epoxies. He found that epoxy-based fluxes could be made with a high level of activity. The flux residue was converted to neutral and non-corrosive polymer during reflow. The residue passed SIR (surface insulation resistance) because the active flux was consumed by the reactive epoxies. The flux agent played a dual role by initially assisting soldering and then serving as the hardener for the epoxy resins. The invention led to a family of epoxy-based liquid fluxes

called ChipFlux 2020 designed specifically for the Flip Chip. This novel approach was granted broad patent coverage [5].

Flux/Underfill

The epoxy-based fluxes soon became the preferred class for Flip Chips because these materials were very compatible with epoxy-based underfill. The polymerized epoxy flux residue bonded strongly to the substrate. The underfill then bonded strongly to the residue. Most likely, the flux and underfill formed a single inter-linked polymer matrix. Researchers asked the obvious question, “Can the epoxy flux and epoxy underfill be combined into a single material?”

Several companies and universities that include Alpha Metals, Georgia Institute of Technology, Kester and Motorola pursued this area of development beginning in the early 1990’s. Many problems were encountered for the pre-applied flux-underfills, but thanks to a long and intensive effort by Professor Dan Baldwin, his students and associates at Georgia Tech, a practical process was developed and reliability data was generated. Today, several companies have or will introduce pre-applied flux-underfill products although the technology has not yet gained wide acceptance.

The pre-applied flux-underfills, also called fluxfills, “no flows” and other obvious names that will likely become trademarks, have limitations that can make them unsuitable for some FC assemblies. First, today’s products are unfilled systems. The addition of inorganic fillers, like silica, interferes with soldering to significantly reduce yield. No filler results in a higher CTE (Coefficient of Thermal Expansion) compared to capillary flow products. The optimum CTE value is a match to the solder joint - 25 ppm/^{o}C. The “no filler” products have values as high as 75 ppm/^{o}C creating more stress. Still, these materials have passed 1000 cycles @ -55^{o}C to 125^{o}C with smaller (0.250” die) [6]. Although the pre-dispensed liquids are not perfect, they bring us much closer to running Flip Chip as a standard SMT process.

[Figure 2 –No Flow Process]

What’s Next for Underfills

How do we take the next step along the road to success in making Flip Chip the ultimate package? Once again, we need to step back to move forward. Several years ago, we began investigating the feasibility of building flux and underfill right into the chip. The materials would need to be solids, preferably “meltable” polymers – from the large thermoplastic class! Thermoplastics have been used in electronic packaging and printed circuits for a long time. Solid die attach films, such as Staystik®, have been used to bond large and small die for the past decade. These low stress thermoplastics have established an excellent record. Significantly, one application method involves wafer-level (W-L) coating with a

solution of die attach adhesive, drying to a solid and then dicing. The resulting ***ready-to-bond*** chips are easily handled and quickly bonded by heat activation. There is no resin, no curing, no chemistry, no surprises - only the simple mechanics of melting, bonding and cooling a pre-polymerized adhesive.

Now back to underfill that is clearly an adhesive. We should note primary purpose of underfill is to strongly bond the chip to substrate and mechanically couple or "lock" the structure together. This is what prevents strain-producing movement within the interconnect region. Why not coat the face of the chip with underfill adhesive? Certainly this is more challenging than coating the back of a wafer, but it is feasible. Let's look back just one more time to discover that there are already **solid** underfills.

RACAs and PACAs

Many observant technologists have remarked that anisotropic conductive adhesives (ACA) eliminate the underfill. Actually, the ACA embodies a built-in underfill. The dielectric adhesive part of the ACA is an underfill. There are two classes of anisotropic adhesives; those with randomly dispersed conductive particles, called random anisotropic conductive adhesives (RACA) and a patterned array type. The second less common type, the patterned anisotropic conductive adhesive (PACA), is really a composite of underfill adhesive with an array of conductive adhesive "islands". In fact, materials have been developed using B-staged silica-filled epoxies as the dielectric. Some of these PACAs have been designed for Flip Chip [7,]. Figure 3 shows a PACA process.

[Figure 3 – PACA Process]

Flipped Underfill = "UnderFlip"

Let's now focus on solid underfill. We now report work on solid flux and underfill intended for wafer-level application to Flip Chip and other array products. Not only should the FC contain the necessary flux and underfill, the finished assembly should be REWORKABLE. This may seem like a tall order since many have tried and failed, but shifting to solid underfill opens up the world of thermoplastics recognized for their practical reworkability. In fact, Staystik thermoplastic die attach adhesives are used primarily for their reworkability feature. Thermoplastics, unlike thermosets, can be repeatedly melted and hardened just like solder. Thermoplastics are the organic analogs of solder and have been called "polymer solders" or "organic solders" [8, 9]. Utilization of thermoplastics as the underfill layer thus bestows the elusive workability feature. Note that pre-polymerized thermoplastics have not been used for capillary flow underfill because they are made into liquids by adding solvent. Solvent evaporation within the confines of an assembled Flip Chip would produce unacceptable voids and shrinkage upon drying.

The W-L flux and underfill coated Flip Chip is now a true SMT package. Our primary approach among a plethora of possibilities has been to keep the underfill and flux layers separate although a single flux-underfill material has been made. There are two reasons for the dual-layer approach. First, it is easier to optimize the individual sets of flux and underfill properties without compromise. Secondly, the underfill, or “underflip” layer, can be filled since this will not interfere with soldering. The flux layer does not have nor does it require filler. Figure 4 shows the dual-layer concept but there are many possibilities including fully surrounding the bumps with flux [10, 11].

[Figure 4 – W-L FC]

The solid flux is a modification of the liquid ChipFlux2020 epoxy system that has been in commercial use for several years. The main challenge was converting resins to solid epoxy and selecting the solvents. The judicious choice of solid epoxy, flux-active hardener, solvent and tackifier allows formulation of coatable flux with an engineered melting ranging from 60^{o}C up to 160^{o}C. The level of tackiness useful for holding the chip in place can be adjusted. The solid version of ChipFlux 2020 is providing good soldering and joint formation. The flux is thermally converted to a strongly bonding inert polymer that can also serve as a primer for the thermoplastic underfill that does not need to melt during reflow. Figure 5 depicts the proposed FC=SMT® process.

[Figure 5 – Reflow Profile from ppt.]

Application Methods

There are several practical wafer-coating methods. Stenciling, one of the successful processes used for die attach pastes, can also be used here. Work at Speedline/MPM and Georgia Tech will define the parameters. However, development continues at SCS/Alpha Metals on spin coating, a process more familiar to the semiconductor industry. Spraying and curtain coating are other possibilities.

Flux paste can be selectively applied to bumps by roller coating or wafer dipping. The wafer dipping approach is similar to the flux application process for single Flip Chips using a rotating drum. The required amount of paste is spread out on a very smooth and planar rotating disk using a precision doctor blade. The solder-bumped chip or wafer is pressed into this reservoir with bumps down and then withdrawn. Bumps become coated with a specific amount of material that is determined by doctor blade height, withdrawal rate, bump geometry and the paste rheology.

Future Work

During the remainder of 1999, work will continue on W-L application methods and SMT Flip Chip assembly at Cookson, Alpha Metals, SCS, Georgia Tech and Binghamton University with materials modification as required. Beta site testing is expected in 2000 and positive results will lead to product introduction in the same year.

Success with this Ready-to-Bond FC concept or any other that enables FC=SMT® will radically enhance the value of Flip Chip. Underfilling will become transparent to the assembler. There will be no extra-step penalties for assembly and the FC will be just another SMD. Triumph over today's underfill limitations will take Flip Chip to the next and final level - a true package [12].

The result: **FC=CSP**.

Reference

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