Wafer-Level Flip Chip Enabled with Solid Underfill

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Abstract

Flip Chip experienced a rebirth and re-engineering during the 1990's from stepped up demands for density and performance that drove packaging to extremes. While developments during the past decade successfully ported FC to low cost organic substrate, the solution to thermomechanical stress has become today's enigma for productivity. Underfill helped solve the chip-to-substrate differential expansion problem but imposed an inhibiting process bottleneck. Flip Chip, originally a very efficient SMT process, is now burdened with the "alien" underfilling step and its significant "productivity tax" that can double assembly cost. What's more, underfilled assemblies are not reworkable - a requirement for a true package.

Total Wafer-Level Flip Chip processing can fully enable the FC to make it an authentic and potentially ultimate micropackage. Developments in coatable solid flux and underfill promise to eliminate board-level processing and bring back reworkability. The ready-to-bond FC will assemble just like any SMD making the underfill process invisible to the assembler. This paper will discuss strategies for WL-FC processing and give an up-to-date status report. Success with wafer-level processing will have a profound affect on Flip Chip. The result: FC = CSP!

Keywords: flip chip, wafer level, underfill, flux, rework, assembly

Introduction

Flip chip has been loved by designers and hated by assemblers for much of the last decade. Designers love this almost ultimate package because nothing is smaller (chip size), can handle more I/Os (>10,000) or has higher electrical performance. Yes, flip chip is almost the perfect package. There are some issues to be sure. Die shrink, where an IC is made smaller during its product life to boost speed and reduce cost, is an issue. Sooner or later, the bump pattern on the FC needs to be changed and that means changing the pad pattern on the circuit board. There are some solutions, but none is perfect. Known good die remains an issue, but wafer-level testing continues to improve and may eventually solve this problem. The bigger issue, of course, is underfill. The materials are reasonable good, but the process is a major annoyance, yet even worse, a productivity detractor. Some suggest that the underfill step cuts manufacturing output in half to nearly double the cost [1]. The small cost of a miniscule amount of underfill for a tiny flip chip is not at issue. It is the PROCESS that needs fixing.

Underfill Materials

CUF

The early underfills were silica-filled liquid epoxies [2]. The modern underfills, nearly 2-decades later, are silica-filled epoxies. It is true that the so-called state-of-the-art materials are lower in viscosity and cure faster, but the process still makes any capillary flow underfill (CUF) undesirable [3]. One must assemble the flip chip to a substrate, allow CUF to flow completely under the chip and often add a fillet to one or more sides. All of this eats up processing time on sophisticated lines. There are alternatives [4, 5].

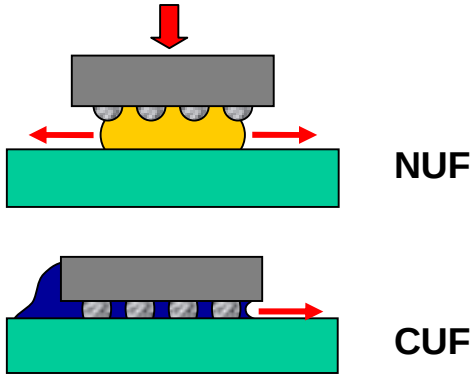

Figure 1 – NUF vs. CUF Processing

NUF

In the early 1990's, technologists at Alpha Metals, working on underfills and flux compared notes. The "fluxologists" were working on a new system with epoxies in search of a better answer to "no clean". The chemists from each group were amazed to find that the new epoxy-based flux and CUF had similar chemistries. They did the obvious and attempted to merge the two systems into self-fluxing underfill that could be pre-applied. One problem became immediately apparent. The presence of silica filler interfered with solder joint formation. The filler dilemma is still unresolved today. Absence of filler

solves the soldering problem but the cured underfill has a higher-than-optimum CTE (Coefficient of Thermal Expansion). Figure 1 compares CUF and NUF processing.

Most now agree that the CTE of the underfill should be similar to that of the flip chip joints, or about 25 ppm/C for common solder [6]. Epoxies have natural CTE values of 70 to 85 ppm/C so unfilled systems produce more vertical stress during thermal cycling. The unfilled underfill expands at a greater rate than the solder joint during heating and contracts more on cooling. Another factor is that shrinkage is greater without filler. The so-called "No Flow" (NUF) underfills are therefore thought to be less reliable than CUF types and assemblers are reluctant to use them for larger chips such as CPUs. But the NUFs are still considered reliable for smaller die and several commercial products have come to market. Figure 2 shows CTE affects on the assembly.

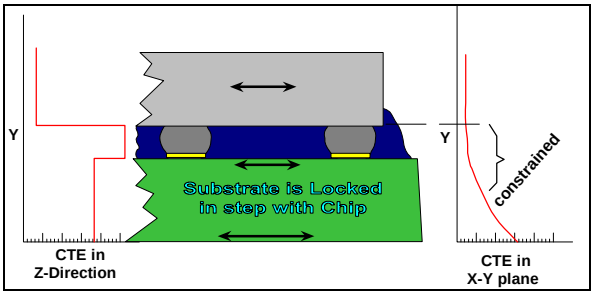

Figure 2 – CTE vs. Stress

There are certainly technical solutions to the silica filler problem. Less filler can be used, but the CTE will not be optimum unless about 60 – 70% silica by weight is used. Figure 3 shows the variation of CTE with silica loading. Some feel that different filler may work better and this may be true. But even if a low-stress NUF is made, it will never be the optimum underfill. Once again, the process is the problem. NUF still needs an added step and extra equipment. The process must be precisely controlled to prevent air entrapment.

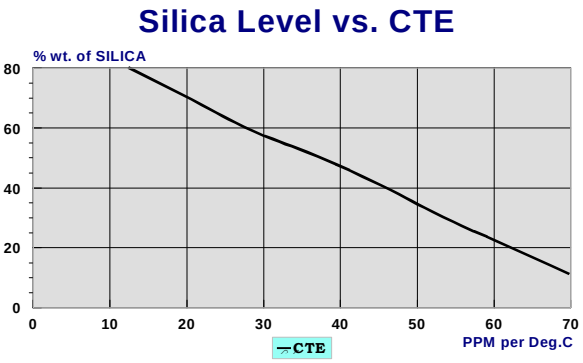

Figure 3 – CTE vs. Silica Level

WUF

Micropackaging is rapidly moving to wafer-level (WL) processing for productivity. Several Chip Scale Packages (CSP) have made the jump. But the principle behind WL is not really new if we look at component assembly. The ceramic, Printed Circuit Board (PCB) and flexible circuit assemblers have typically tried to leave a multi-up array of circuits in tact until assembly and test was completed [7]. A large panel array of perhaps hundreds of individual circuits (if the circuits are small) can be screen-printed with solder paste, populated with SMDs, reflow soldered, tested and then singulated or depanalized. Running the packaging processes on a wafer makes sense. While the analogy between 2nd level assembly and first level may be interesting, a look at micropackaging will show that true wafer-level manufacturing has been around long before CSPs went that route.

Wafer-Level Flip Chip

Flip chip bumping has been a wafer-level process for about 3 decades. In fact, most Under Bump Metallization (UMB) and bumping processes won't even work on single chips. The original vacuum-deposited IBM C4 process was certainly wafer level. Newer plating methods are WL as is solder paste stencil printing for bumping. So why not run the underfilling process at wafer level? A bumped or even an unbumped wafer can be coated with underfill by a number of well-known methods. Stenciling, screen-printing, spin dispensing and curtain coating have all been considered. Some of the methods have obvious problems [8, 9]. Screen-printing tends to leave screen mesh marks and has a maximum thickness limit that can be inadequate especially if a lower solids solution is printed. Screen-printing can also damage bumps. However, others seem committed to making this process work for wafer coating. Spin coating can have a problem with bump shadowing as center-deposited liquid radiates out to the wafer perimeter. However, a leveling step can overcome this problem.

We have had reasonably good results using stencil printing equipment from Speedline who make printers designed specifically for wafer printing although initially intended for bumping. Stenciling can apply substantial thickness of material, well beyond the requirements for underfill. The use of an open stencil precludes any possibility of bump damage. And since stencil printing has been used to apply die attach adhesive to the back of wafers, there is a wealth of knowledge available. Figure 4 shows a wafer that has been stencil-coated with polymer.

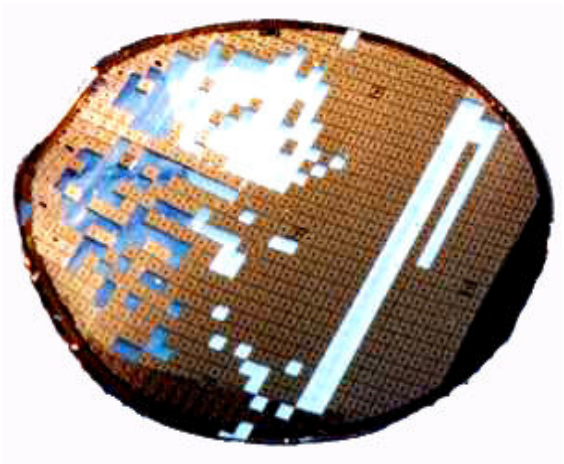

Figure 4 – Staystik Coated at Wafer-Level

We are now faced with a material phase issue. Flowable liquids and thixotropic pastes are convenient and even ideal forms for application. But the liquid phase is not practical for further processing, handling and eventual shipping. The final form of the wafer-level underfill (WUF) must be a solid. The caveat is that the solid must be capable of returning back to a liquid phase during the flip chip assembly step. Note that the solid does not have to become a low viscosity fluid. A softened deformable state is sufficient for bonding. Adhesion requires that the bonding material wet out the substrate. There are several approaches for achieving solid underfill that can be bonded at a later stage.

Solid Underfill Systems

There are two fundamental types of polymers, thermoset and thermoplastic. Thermosets, as the name implies, are "set" or polymerized into a non-melting relatively permanent form. The thermosets can start off as a free-flowing liquid, but once hardened, they retain shape due to the molecular structure. The thermosets have shape-retaining "memory" and very good properties. The thermosets are therefore the "work horse" polymers of electronics. They are used in nearly everything, including PCB laminates, liquid encapsulants, molding compounds and, of course, underfill. Although thermosets can be polymerized to a fully cured stage (C-stage), some can be partially polymerized. The process of bringing a thermoset to a partial cure that permits full curing later is called B-staging. The resin system is allowed to come to a low level of polymerization, called the B-stage, which yields a solid that can be melted by heating. Let's now look at the thermoplastic type of polymer and then return to B-staging concepts.

Thermoplastics

Thermoplastics are mostly linear chains of atoms that are long enough to be solids. Longer chains, and subsequently higher molecular weight, produces higher melting materials. Generally, the higher the molecular weight, the higher the melting point. Liquefaction requires addition of energy in the form of heat to bring molecular motion to a level where molecules can move independently and change the shape of the mass. The thermoplastics, unlike the thermosets, do not have cross-links between chains as shown in Figure 5. The thermoplastic polymer chains can move independently once enough heat, or thermal energy, is applied to give them adequate motion and the mobility we observe in liquids. The thermosets have intermolecular links, or chemical bonds, that prevent the chains from sliding past one another. We can look at a mass of cured thermoset as one giant molecule since all of the polymer chains are connected together by the cross-links. A thermoset underfill that is fully cured cannot be melted and would not bond to substrate. The cross-links permanently lock in the shape – hence molecular memory.

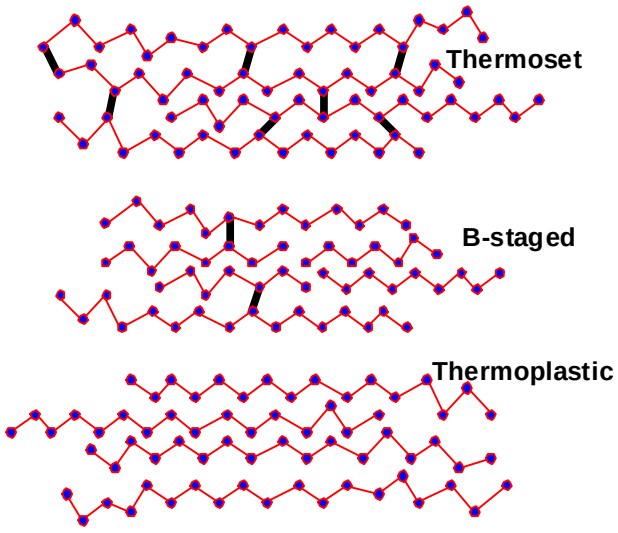

Figure 5 – Polymer Types

B-Staged Polymers

Let's now return to B-staged polymers since they can be useful for wafer-level underfills. We can produce a B-staged system by allowing polymerization to only proceed to a level where the material has just solidified. We can liquefy the material again by raising the temperature of the B-staged product. As mentioned before, bonded to substrate typically requires returning to a liquid phase. Once bonding has occurred, the B-staged polymer can then be fully cured by additional heating. Most chemical reactions are accelerated (doubled for every 10^{o}C rise) by

increasing the temperature and this applies also to B-staged systems. This means that the B-staged polymer can first melt and then fully cure during the reflow soldering process if correctly catalyzed. This is the principle of B-staging. Figure 5 compares B-staged to thermoplastic and thermoset. The B-staged system is sometimes a hybrid since there may be a few cross-links, but a well-designed system will be mostly linear and behave like a thermoplastic. Thus, a thermoset in it's A-stage, could be applied to the wafer, polymerized to B-stage and then brought to final C-stage on assembly.

Solid A-Staged Systems

While B-staged polymers can be used for solid underfill, a simpler approach is to start with solid resins and hardeners. Many thermoset resins are solids at room temperature, but melt when heated. The same applies to hardeners that are used to polymerize these resins. A thermosetting underfill can therefore be made with solids (A-stage) that will melt, bond and then fully polymerize. This is the principle used for epoxy molding compounds (EMC) that are used for most of today's plastic packages. The EMCs are used as solids, often called hockey pucks that are melted, injected into molds and then cured.

Although a low melting EMC type system could be melted and coated onto a wafer, we have found that a solvent solution is more versatile. The resin, hardener and catalyst can be dissolved in solvent that can be wafer-coated by the methods mentioned earlier. Filler can be included if a separate flux level is to be used. The underfill can be designed as a paste with the right rheology for nearly any coating method. Evaporating the solvent then hardens the wafer coating. The solid can be heated to its melting point for bonding during FC assembly. Melting can be designed to occur over a range from about 50^{o}C to over 130^{o}C by proper choice of resins and hardeners. The catalyst is selected to allow polymerization to be completed during solder reflow. Alternatively, a system can be designed so that the solder assembly process only brings the underfill to a B-stage. This would permit rework but add a post-bake step. While the solid underfill can be made self-fluxing, a separate flux layer can now be added.

Thermoplastic Underfill

A third strategy is to use a thermoplastic polymer. Many thermoplastics can be dissolved in solvent, coated as a liquid and then dried back to the same solid without any change in properties. The thermoplastic can be bonded to a substrate by heating to its softening point. In fact, there is already a precedent for using thermoplastics on bare die. Staystik^{TM} thermoplastic die attach adhesives have been used for many years to bond die to PCBs and packages [10]. The material is commonly used as a film that is placed between die and substrate. However, some packaging assemblers have used a paste version or a low viscosity solution to coat wafers. The material is applied to the back of a wafer, dried to a solid by solvent evaporation and then the wafer is diced as shown in Figure 4. The presence of polymer on the wafer does not interfere with sawing to any great extent. The wafer must be kept cool and the adhesive should have a reasonably high melting point for sawing. Once the wafer is sawn, the die can be handled and shipped. Storage is at room temperature and these kinds of materials have a very long lifetime. Bonding requires heat although pressure is typically used to allow bonding at a lower temperature.

The same concepts can be used for underfill with two differences. The filler cannot be electrically conductive and the coating is applied to the front, or active side of the wafer. Sawing is more problematic, but a method has been developed that overcomes any difficulties. The dried thermoplastic underfill can contain fluxing agents, but a separate flux layer is preferred. The use of thermoplastic polymers allows reworking. The Staystik die attach adhesives are used primarily for their reworkability. Application of heat and torque permits die to be removed and the adhesive layer can be cleanly peeled away. Reworking is more complex for flip chips because of the presence of joints, however.

Flux

Just like NUF, WUF requires fluxing properties or a separate flux layer must be added to the wafer. One value of a solid underfill system is that separate layers can be formed unlike NUF or CUF that are inherently single-layer concepts. While polymer systems can be activated to have fluxing properties, our work has shown that there are significant benefits in keeping the flux as a distinct layer. A two-layer underfill and flux system allows each to be optimized. A more important benefit is that the underfill layer can be filled and the flux layer can be kept unfilled. The flux layer, that is obviously the last one applied to the wafer, can be designed to act as a primer so that the UF layer doesn't need to liquefy. Filler is not as important for the flux layer since it makes up only a small part of the UF/flux system. There is much wider latitude for fillers in the WUF system since material does not have to flow between chip and substrate as with CUF. Thermally conductive fillers are possible.

Our earlier work in epoxy-based fluxes [11] has led to solid systems that can be coated from solution and dried. Upon exposure to reflow solder temperatures, the liquefied material will polymerize to a thermoset with strong bonding properties. Some work has been done on a system that forms a thermoplastic-like solid after reflow, but suitable cured properties have not yet been achieved.

FC = CSP?

While others struggle with redefining the term CSP, we suggest that a flip chip that contains flux and packaging material is really a CSP. Some definitions require that the package is removable and maybe reworkable, but this may be possible with thermoplastic underfill. The final package is essentially formed during the solder assembly step. The underfilling step, when performed at wafer-level will no longer concern to the assembler. And depending on the polymer system used, the underfill can be reworkable. Figure 6 shows the WL FC concept. Flux can be applied to bumps only or the entire underfill surface.

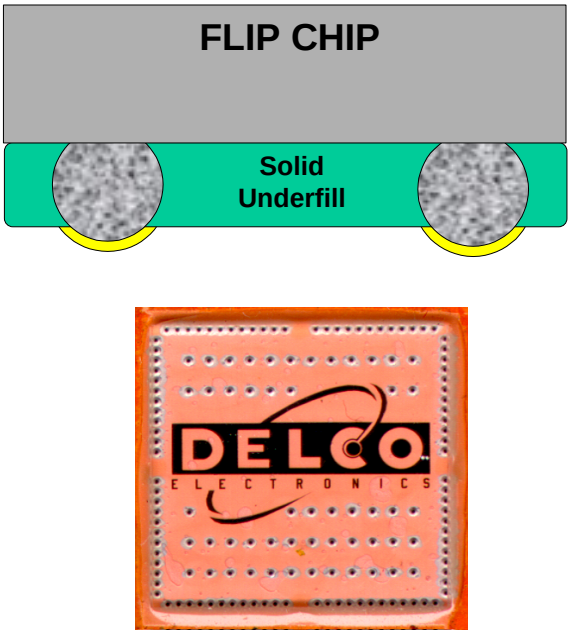

Figure 6 – WF-FC (Quartz FCs supplied by Delphi/ Delco Systems)

WUFed FCs?

A wafer-level coated flip chip is a *ready-to-bond* SMD. The flip chip with dry flux and underfill can be placed in tape & reel or waffle packs. Significantly, the FC assembly process is back in the realm of SMT. In fact FC = SMT. WUFed FCs appear to be the ultimate micropackage since nothing can be smaller, faster or simpler.

But where is the wafer-level flip chip? While most believe that such a system will eventually succeed, no commercial products have been introduced. Although several companies, universities and consortia are working in this area, much work remains. Possibly, a product will be commercialized this year, but there are no guarantees.

Conclusions

While a few state-of-the-art underfills flow rapidly and cure in about 5 minutes, the time and equipment penalty required for underfilling limits flip chip technology. Solid flux/underfill systems can and should be made an integral part of the flip chip to smash the underfill "bottleneck". A reworkable system is desirable although not essential.

A WUF flip chip will be a true package, likely a CSP that will take advantage of the SMD infrastructure. Work in this field has gone far in demonstrating the feasibility of solid underfill/flux. Continued work in this area can be expected to produce the desired system that will have major ramifications for the packaging industry. A move to wafer-level converts the flip chip to a assembly-friendly CSP and allows in-line high-speed production. Underfill is thus moved from board-level application to semiconductor processing. However, no commercial product has become available and the timetable is still indefinite.

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