Polymer Materials
The Empowerment of Flip Chips

By

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Abstract

FASTER, SMALLER, CHEAPER is catapulting packaging technology to its limits. Flip Chip is being positioned as the ultimate packaging solution. Transformation from standard chip & wire assembly to flip chip brings important benefits to the entire electronics industry. Flip Chip technology completely removes interconnect wires to create shorter paths for the highest electrical performance possible. The package profile shrinks to the absolute minimum, the footprint becomes chip size and the cost curve drops to the lowest possible potential of any technology. Flip Chip on organic substrates, FR-4, BT, and flexible circuitry are becoming the norm. Yet, the transition of flip chip from ceramic to organic substrate is causing CTE mismatch problems that challenge reliability performance. Efforts now focus on eliminating thermomechanical fatigue while boosting productivity and lower manufacturing costs. Reliability is not sacrificed

Several advances in recent years have moved polymer encapsulating and joining materials to the forefront of flip chip technology. Underfill is the material that enables the flip chip to perform at a high reliability level on low cost substrate. Underfill reduces mismatch stress of the flip chip interconnect to provide long-term thermomechanical and environmental reliability for virtually any application. Introduction of new fluxing technologies allow the manufacturer to mount the flip chip onto the substrate and not have to consider the possibly of the flux contaminating the underfill process. Finally, the concept of removing the solder altogether from the bumping process has already materialized. Replacing the material with low cost electrolysis nickel and attaching the package with silver filled epoxy will simplify production further.

Flip Chip is the original SMT product, the first Chip Scale Package (CSP) and also the first ball grid array (BGA) that has served the computer and automotive industries so well for many decades. A re-engineering of this eloquently simple approach to minimal packaging now brings flip chip to the affordable range of customer electronics. Indeed, this approach is now being utilized by corporations for large-scale production. This paper will investigate the critical joining materials elements that include bumping, joining and underfilling flip chip packages. We will also gaze into the future of flip chip interconnect materials which will ultimately lead flip chip technology to high density, high performance electronic packaging.

Introduction:

Modern electronics is primarily based on solid-state integrated circuit technology that can range from simple devices to amazingly complex computer chips that surpass the performance of many supercomputers. Semiconductor technology continues to advance at a relentless pace. Processor speeds of ICs are typically boosted by shrinking the size of the chip in order to reduce signal path lengths within the device. The chip "shrink" allows higher clock rates (megahertz rating) to run which directly translates to higher processor output. Performance is also boosted by increasing the number of transistors per chip. Powerful computer chips now contain millions of transistors that require more connections (I/Os) to the outside world. The combination of reduced chip real estate, more I/Os and faster clock rates continues to put excessive demands on packaging and board-level interconnection technologies.

A crucial juncture was reached during the 1990's when electronics hit a performance plateau where the conventional SMT package was no longer adequate for some applications. The situation can only worsen in the future as more of us march to the beat of the faster-smaller-cheaper theme.

The Packaging Dilemma

The electronic component package is generally viewed as a housing that protects a solid-state device from the environment while facilitating testing, handling, and board level interconnection. But there is an often-overlooked downside. The package:

- Significantly increases footprint size
- Increases height
- Adds considerable weight
- Degrades electronic performance
- Often serves as a moisture trap that requires added processing steps
- Adds cost

The basic design of the most common SMT packages has an intrinsic flaw. Interconnect real estate is inefficiently utilized. Most packages today, use a perimeter lead configuration wasting up to 90% of the available area. The wasted area in perimeter I/O packaging was mostly ignored until a few years ago. Chip designers continued to increase the number of I/Os while packaging engineers reduced the packaging size. With I/Os climbing and package perimeter declining, it was inevitable that SMT perimeter package become impractical for some ICs. Figure 1 illustrates the wasted board space.

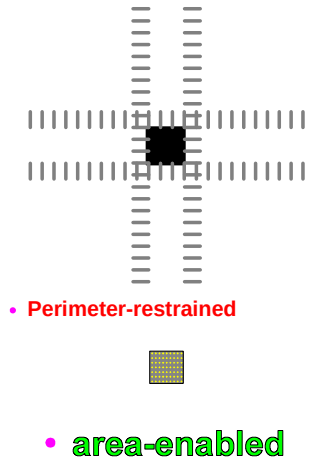

Figure 1. Misused Real Estate

The obvious solution was the area array package exemplified by a plethora of Ball Grid Array (BGA) designs. The BGA package is certainly a concept whose time has come. Taking the process to its obvious conclusion results in the concept being applied to a bare die. An area array chip in Ball Grid Array format should provide an extremely simple system having a smaller footprint, lower profile, higher performance and lower cost than the "new" BGA products. Perhaps the chip-BGA would be the ultimate package. For the answer, we need to move back in time by more than 30 years.

Enter the Flip Chip

While many wondered about the impact of the newly invented transistor, others understood where the early road map of solid-state electronics was to take the world. Jack Kilby, a taciturn, but tenacious engineer at Texas Instruments, realized that transistor-level integration was the first prerequisite to enable solid-state electronics. The successful development and implementation of the integrated circuit (IC) by TI, Fairchild, Intel and others, created the need for more complex packaging. The new semiconductor companies tackled the problem and introduced numerous solutions. Wire bonding and direct lead frame bonding (spider circuits) gained headway and became mainstream technologies that are still in use today as chip & wire and TAB (Tape Automated Bonding).

In another camp, located in the beautiful campuses of upstate New York, the worlds' largest computer company took a more direct approach. Why not solder the chip to the circuit board? The technology was simple and straight forward. Significant developments in materials and processes would be needed, however, but IBM had the horsepower to deliver the needed technologies.

IBM's first successful implementation of direct chip attach (DCA) involved soldering copper balls to the IC pads somewhat analogous to today's BGA construction. Alpha Metals produced billions of micro-spheres for IBM to build the new flip chip packages. This package is displayed in Figure 2.

1964 FLIP CHIP

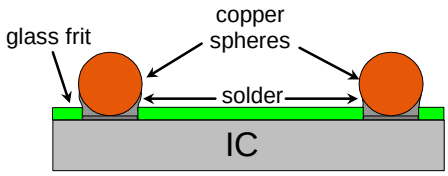

FIG. 2

Figure 2. 1964 Flip Chip

The flip chip moniker resulted from the need to flip the chip over, or face down, for assembly although some may argue that wire bonded chips are upside down. IBM continued to use the copper ball technology while searching for higher productivity methods. The scheme finally selected was vacuum deposition of tin-lead solder. Solder was deposited through a mask to form columns that were reflowed into spherical bumps. The process achieved good productivity since deposition was carried out at wafer level. The bumped flip chip was named C^4 for Controlled Collapse Chip Connection. The difficulty in typing the exponent "4" led to today's term, C4 (Figure 3). The C4 process has served IBM and other mainframe builders for decades and this direct chip attach (DCA) method holds the record for reliability.

Figure 3. Original C4 Flip Chip

Enter the "Faster, Smaller, Cheaper" (F-S-C) paradigm. The need to reduce size and increase performance while holding the line on cost, has put tremendous pressures on packaging. In fact, the challenge has so overwhelmed conventional SMD packaging technology that we have been launched into the Packaging Revolution. One of the

important elements of this revolution is the move from perimeter-restraining connections to area-enabling designs. Package downsizing is another important element which is made easier by area array concepts. Size reduction can be expected to move us to chip-scale and finally to the "packageless" package. Figure 4 shows this growing proportion of flip chips in package assembly. Indeed sized reduced packages are carving out their own niche in the growing microelectronics industry.

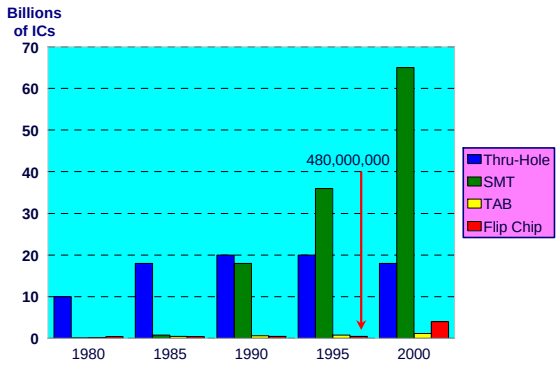

Figure 4. Future Trends for the Microelectronics Assembly

Flip Chip Assembly

There are two basic types of assembly processes for flip chip: (1) joining material contained in bumps and (2) joining material applied to bump or circuit pads. Eutectic solder bumps allow assembly by simply reflowing the bump and allowing it to form a junction with the circuit board pads. Solder paste can be used where the bump is not readily fusible. High melting C4 bumps can be used with eutectic solder paste to allow reflow to occur at normal SMT processing temperatures. Solder paste can also be used for attaching electroless nickel bumps currently being offered by Flip Chip Technologies.

Flux is typically applied prior to chip placement. Flip chip flux can be applied to the solder bumps using an automatic fluxer, or to the circuit by a number of methods. "No clean" fluxes are now available that have been specifically designed for flip chips. The newer generation fluxes are now epoxy based. Epoxy-based fluxes undergo a severe drop in viscosity during reflow. Organic acids within the flux clean the surfaces and wet the solder to the interfaces. The epoxy flux then cures into an inert material as the reflow stage concludes. There is no detrimental residue left behind. No cleaning is necessary since the flux material is itself epoxy based and is totally compatible with the underfill material. This harmony makes epoxy base fluxes the ideal choice for flip chip solder attach.

Although touted as a replacement for solder for surface mount, conductive adhesives lost their steam as the "green revolution" ground to a halt. However, conductive adhesives are beginning to gain new life as flip chip joining materials for nickel bumps as well as gold stud bumps. A conductive adhesive offers several advantages over traditional

eutectic solder. Cleaning and fluxing are now eliminated from the process. Problems an operator may have had with these materials have now been eliminated. Conductive adhesives are also fully chemically compatible with underfill materials. Furthermore, the removal of lead eliminates the worries of α particle emission that plague memory devices. Lastly, silver filled epoxies have the capabilities of very fine pitch. The impetus of faster-smaller-cheaper can possibly drive pitch between flip chip bumps past the limits of current solder technology. Of course, one should not forget the environmental friendliness of using epoxies over solder although, admittedly, that issue seems to have faded into the sunset.

One important new process, which we call "Polymer Dip Chip" (PDC), involves dipping the bumped chip into a reservoir of conductive adhesive so that it coats the bumps. The chip can now be placed onto the circuit and the adhesive hardened with heat. The PDC process offers simplicity and avoids having to selectively apply adhesive by screen printing or stenciling. The only registration step is in the placement of the chip onto the circuit.

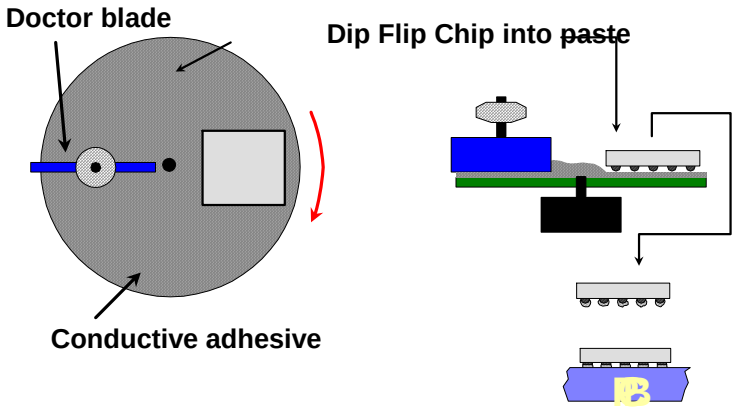

Figure 5. Polymer Dip Chip Process

Underfill Materials

Figure 6 is a cross section of an underfill material. Let's demystify the often-maligned underfill which is accused, by purveyors of alternate packaging, of being the bottleneck and anathema of flip chip on organic boards. Underfill is simply a mineral-filled adhesive composite that is placed between the circuit board and the bonded chip. Some companies have installed in-line setups and are in high volume production now. This point is reinforced by Figure 7 - a circuit board from a consumer Handycam. Most of the IC's are assembled flip chips. Clearly, flip chips can be incorporated into assembly and still meets the rigors of the consumer market.

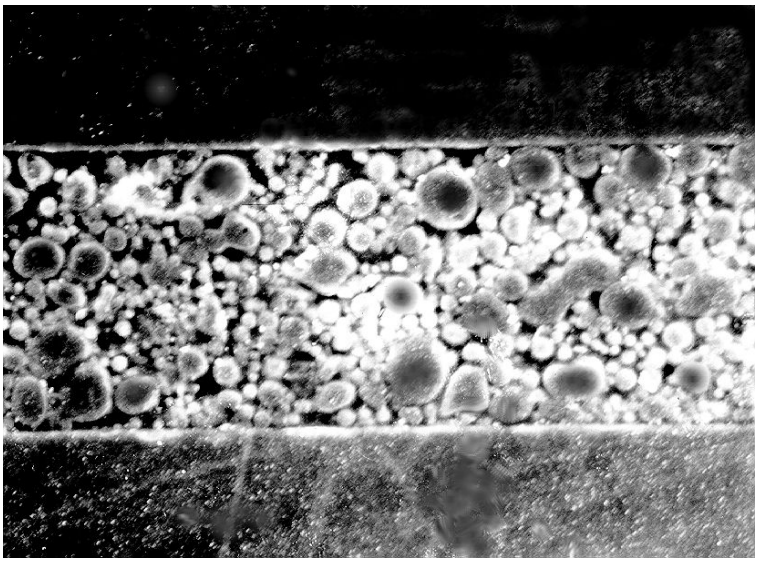

Figure 6. Underfill Cross Section

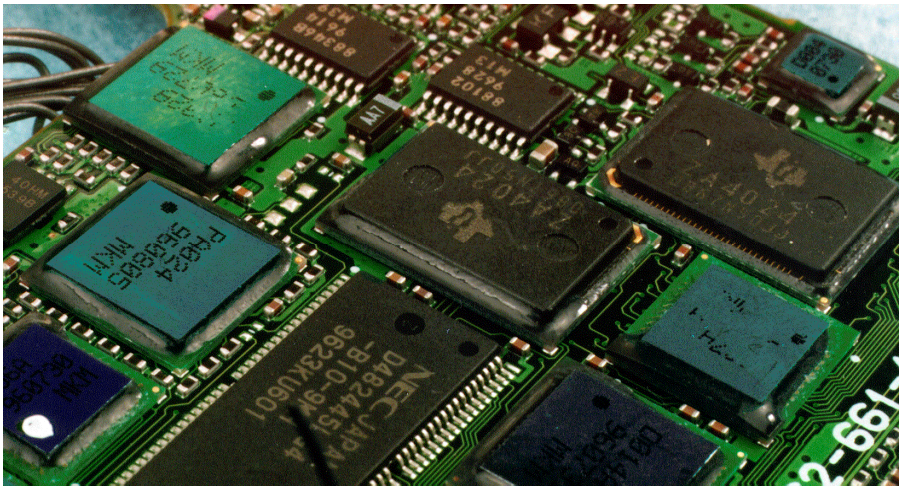

Figure 7. Handycam Circuit Board

Underfill is dispensed on one or two sides of the chip. State-of-the-art products can flow under a typical 250-mil die in a few seconds. The fluid material is flowed under the chip gap by capillary action after assembly and test. A fillet can be optionally formed by applying more underfill opposite to the sides of the die where initial dispensing occurred. The underfill is then hardened into a structure that boosts thermocycle performance to an acceptable level. Figure 8 is a simple diagram of the process.

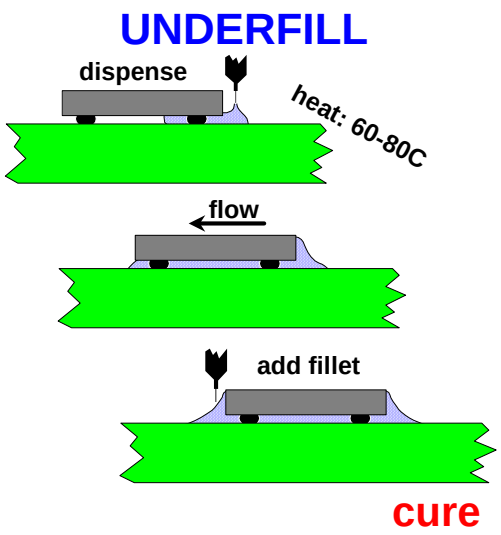

Figure 8. The Basic Underfill Process

As pointed out earlier, the problem with bonding a silicon device directly to an organic circuit is that severe thermomechanical stress and fatigue will result. The circuit board will expand and contract at a much higher rate than the silicon during each thermal cycle. The joining material, such as the solder bumps on the flip chip, will experience work hardening and embrittlement as it is deformed during thermal cycling. The very low bump height (1 - 4 mils) accentuates the problem by concentrating stress. Reliability is low and the construction is really not a viable technology.

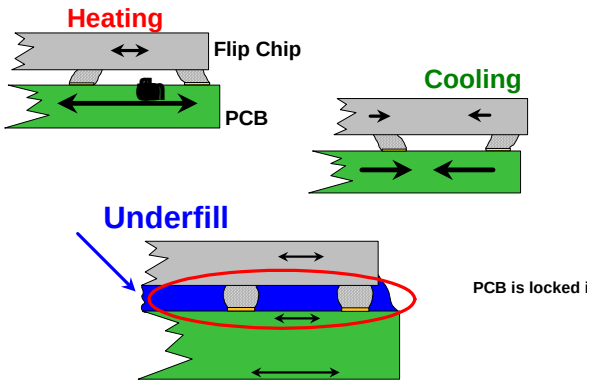

Figure 9. Underfill Locking Action

The cost-effective solution of adding underfill between the flip chip and circuit board boosts reliability by an order of magnitude or more. The simplest explanation for the outstanding results is that the hardened underfill locks the board movement to that of the silicon chip (Figure 9). The low expansion, very high modulus inorganic silicon becomes the restraining force that restricts the expansion of the organic circuit board, at least at the surface. The underfill must be a relatively stiff, high modulus material to lock the silicon

and PCB together. The expansion coefficient of the underfill should be close to that of the joining material, 25 ppm/^{o}C in the case of solder. If the Coefficient Temperature of Expansion (CTE) of the underfill is too high or low, vertical stress will result and the joint will fail. The CTE can be easily adjusted by adding mineral filler to the polymer system.

Emerging Products

Using one type of underfill for every application is like using one golf club for the entire round. There are no standards in the industry for flip chip package designs. Consequently, many manufacturers are customizing their products for specific customer demands. Although underfill products have made great strides in the past year, new concepts are being developed and some are even in the final stages of testing on real assemblies. One of the most valuable recent developments during 1995 - 1996, was the introduction of fast processing underfill. The flow rate has been increased by an order of magnitude and the cure time has been cut by 1/4th. The typical flip chip used for cellular products, for example, can be underfilled in less than 15 seconds with a cure schedule of 1/2 hour or even less. Materials in 1997 are expected to decrease cure to 15 minutes. The old complaint that the underfill step is high cost and time penalty is no longer valid.

Some of the more exciting anticipated developments are underfill products with these features alone or in combination:

1. Stress-relief underfill with thermoset-thermoplastic characteristics
2. Self-filleting
3. Self-fluxing
4. Self-fluxing underfill film applied at wafer level
5. Visual cure indicator

Stress-Relief

Stress-relieving underfill is already on flip chip products. How does it work? The underfill begins as a low viscosity liquid that is readily flowed under the flip chip. The material is thermally cured to a rigid, high modulus solid that protects joint integrity. The unique base chemistry then puts an unfamiliar twist into the properties into the encapsulant. At a higher temperature, but within the range of thermocycling, the modulus drops by several orders of magnitude allowing the underfill to behave like a thermoplastic that allows stress to be relieved. The *intrinsic stress relief* (ISR) underfill can have a T_g below the thermocycling range apparently in violation of the old rule that states the glass transition temperature should be very high. The T_g for ISR underfill is someone insignificant because the CTE above and below the T_g is nearly the same; $\alpha_1 \sim \alpha_2$. Standard underfills require a high T_g because expansion above T_g is typically 3 or 4 times higher than below T_g; $\alpha_2 >>> \alpha_1$.

Self Fluxing

Epoxy-based flux is now being used for SMT and flip chip assembly and such products are commercially available worldwide. We and others have found that epoxy-based flux can be modified to provide underfill properties. Conversely, underfill cured with acidic type hardeners possess intrinsic fluxing characteristics. However, the dual-purpose systems tend to compromise both flux and underfill performance while also eliminating reworkability. While self-fluxing underfill continues to be an exciting concept, we anticipate niche applications only.

Wafer Level Flux

Our experience in wafer-level application of dry-bondable die attach adhesives has led to the investigation of dry film underfill. Conceptually, it is possible to coat a bumped flip chip wafer with self-fluxing underfill that can be staged to a dry film. The diced wafer could be packaged in tape in reel or other SMT format. Assembly of the ready-to-bond flip chip would involve picking and placing the device and applying heat by means of a reflow oven. The underfill-flux would convert to a liquid at a suitable temperature, flux constituents would be activated, solder reflow and joint formation would occur and the material would set into a permanent underfill solid. Success in this area would allow flip chips to be processed on standard SMT lines without even having to apply solder or flux. What could be simpler?

Reworkability

Reworkable underfill will become available in the future, perhaps combined with self-fluxing material. However, underfill suppliers are still accessing that need of such a product in the general flip chip market.

Cure Indicators

Many reactive products have been developed that give visual indications of status. It is likely that underfills will become available that provide a color cue to indicate full cure. This feature would serve as a safety check that the process remained within control limits.

Conclusions

Flip chip technology represents the ultimate in package simplicity while offering the highest density and optimum performance. Once the exclusive domain of big computers, flip chip has been re-engineered to an affordable package well suited for the consumer electronics market. Flip chips are now being used in disk drives and cellular phones. More than one hundred companies worldwide are developing flip chip technology. Greasing the skids of the revolution are the polymer joining materials which take the technology to new heights of performance. These polymer materials empower flip chip devices to the forefront of the packages revolution.