Device/Package/PCB/System Technology Categories (2005)

1.0 DEVICES / BACKEND

- 1.1 Electronic only – conventional ICs
- 1.2 SoC (System on Chip)
- 1.3 MEMS
- 1.4 Sensors (MEMS and other)
- 1.5 MOEMS
- 1.6 Optoelectronics devices
- 1.7 Organic Semiconductors
- 1.8 Nanoelectronics [includes some of 1.7]
- 1.9 Processes (after device mfg.)
  - 1.9.1 Wafer thinning
  - 1.9.2 Capping (for MEMS)
  - 1.9.3 WLP (Wafer Level Packaging) [can be split out]
  - 1.9.4 Special Passivation
    - 1.9.4.1 Inorganic
    - 1.9.4.2 Organic (incl. Low k)
    - 1.9.4.3 Bumping – see under Packaging

2.0 PACKAGING (Design & Fabrication)

- 2.1 Packaging by Construction/Type
  - 2.1.1 Feed-Through Plastic (DIP)
    - 2.1.1.1 Plastic overmolded
    - 2.1.1.2 Ceramic/metal
  - 2.1.2 Surface Mount Technology (SMT) Plastic Non-Hermetic
  - 2.1.3 Cavity Style
    - 2.1.3.1 Metal Full-Hermetic
    - 2.1.3.2 Ceramic Hermetic
    - 2.1.3.3 Combined Plastic/Metal/Ceramic Non-Hermetic
    - 2.1.3.4 Injection Molded Plastic Near-Hermetic
  - 2.1.4 Area Array Packages by Material
    - 2.1.4.1 Organic; thermoset & thermoplastic
    - 2.1.4.2 Metal
    - 2.1.4.3 Ceramic
  - 2.1.5 Area Array Packages by Interconnect Type
    - 2.1.5.1 Land Grid Array
    - 2.1.5.2 Ball Grid Array, solder balls
    - 2.1.5.3 Ball Grid Array, non-fusible balls
    - 2.1.5.4 Ball Grid Array Polymer Bonded
    - 2.1.5.5 Pin Grid Array
  - 2.1.6 Chip-Scale Packages (CSP) – many ways of subcategorizaing
    - 2.1.6.1 Routing on chip
    - 2.1.6.2 Routing on substrate
  - 2.1.7 Wafer-Level [can go under devices]
  - 2.1.8 Multichip - MCM/MCP
    - 2.1.8.1 Stacked die; 3D
    - 2.1.8.2 SiP
    - 2.1.8.3 Single plane
    - 2.1.8.4 Multi-plane
    - 2.1.8.5 Combination
    - 2.1.8.6 Stackable Packages
- 2.2 Packaging by Application
  - 2.2.1 Power Packaging

- 2.2.2 RF/microwave
- 2.2.3 LED
- 2.2.4 Optoelectronics
- 2.2.5 MEMS
- 2.2.6 MOEMS
- 2.2.7 Optoelectronics – Photonics
- 2.2.8 Fluidic; fluid-handling
- 2.2.9 Biological interface (bio-med)

2.3 Direct Chip Attach (Flip Chip) – this could go in Bare Die Assembly
- 2.3.1 Bumping
  - 2.3.1.1 Solder; lead-free
  - 2.3.1.2 Solder; low alpha-particle
  - 2.3.1.3 Conductive adhesives
  - 2.3.1.4 Pin/post; formed at wafer level
  - 2.3.1.5 Spring type (FormFactor)
- 2.3.2 Photomasks/insulators
- 2.3.3 Routing
- 2.3.4 Underfill
  - 2.3.4.1 Pre-applied liquid; no flow
  - 2.3.4.2 Pre-applied solid – WUF
  - 2.3.4.3 Post applied – capillary type
- 2.3.5 Joining material for non-fusible bumps

2.4 Direct Chip Build Up on Chip Interconnect; Intel - BBUL, GE system

2.5 Package Platforms/Chip Carriers
- 2.5.1 Lead frames
- 2.5.2 Rigid
  - 2.5.2.1 Organic
  - 2.5.2.2 Ceramic/inorganic
  - 2.5.2.3 Metal
- 2.5.3 Flexible
  - 2.5.3.1 TAB/TCP
  - 2.5.3.2 Fan out BGA (TBGA, Flex-BGA)
  - 2.5.3.3 Fan-in CSP
- 2.5.4 Special – Low k

2.6 Chip Assembly Processes
- 2.6.1 Die attach
- 2.6.2 Wire bonding
- 2.6.3 Flip Chip
- 2.6.4 Pin/post

2.7 Packaging Protection/Enclosures
- 2.7.1 Plastic Encapsulation Materials
  - 2.7.1.1 Reduced flammability
  - 2.7.1.2 Hermeticity class
  - 2.7.1.3 Moisture barrier enhancement
- 2.7.2 Metal
- 2.7.3 Ceramic
- 2.7.4 Thermoplastic Injection Molding

2.8 Package Additives
- 2.8.1 Getters
- 2.8.2 In-package fluids/gels
- 2.8.3 Lubricants; antistiction
- 2.8.4 Other

2.9 Package Manufacturing Processes
- 2.9.1 Lead frame fabrication
- 2.9.2 Chip carrier fabrication
- 2.9.3 Overmolding

- 2.9.4 Hermetic cavity lid sealing
- 2.9.5 Injection Molding
  - 2.9.5.1 Overmolding
  - 2.9.5.2 Cavity molding

3.0 RELATED TECHNOLOGIES

- 3.1 Thermal analysis/management
- 3.2 Electrical characterization
- 3.3 Reliability
- 3.4 CAD
- 3.5 Modeling; FEA, other

4.0 PRINTED WIRING BOARDS - PWB (Design & Fabrication)

- 4.1 Designs/Constructions
  - 4.1.1 Single-sided
  - 4.1.2 Single-sided – double-access
  - 4.1.3 Double-sided
  - 4.1.4 Multilayer
- 4.2 Substrate
  - 4.2.1 Rigid
    - 4.2.1.1 Organic
    - 4.2.1.2 Ceramic
  - 4.2.2 Flexible
    - 4.2.2.1 Adhesive laminate
    - 4.2.2.2 Clad adhesiveless
  - 4.2.3 Copper Foil
    - 4.2.3.1 Bond enhancement
    - 4.2.3.2 Morphology/microstructure
  - 4.2.4 Flame retardants
  - 4.2.5 Reinforcement
  - 4.2.6 Thermal core
- 4.3 Processes
  - 4.3.1 Substrate preparation
  - 4.3.2 Patterning
    - 4.3.2.1 Subtractive; etching
    - 4.3.2.2 Semi-additive
    - 4.3.2.3 Fully-additive copper
    - 4.3.2.4 Fully-additive PTF
  - 4.3.3 Hole/via formation
    - 4.3.3.1 Mechanical drilling
    - 4.3.3.2 Mechanical punching
    - 4.3.3.3 Laser drilling
    - 4.3.3.4 Plasma etching
    - 4.3.3.5 Chemical milling
    - 4.3.3.6 Photoimaging
    - 4.3.3.7 Printing (hybrid circuits and PTF)
  - 4.3.4 Vertical (through-substrate) connections
    - 4.3.4.1 Plated Through-Hole
    - 4.3.4.2 Direct copper plate
    - 4.3.4.3 Conductive plug
  - 4.3.5 Via filling
    - 4.3.5.1 Conductive filler
    - 4.3.5.2 Dielectric filler
  - 4.3.6 Finishing
    - 4.3.6.1 Metal plating
    - 4.3.6.2 OSP

- 4.3.6.3 PTF (Polymer Thick Film)
- 4.3.7 Embedded Passives (can also fit 5.0)
- 4.3.8 Shielding; EMI, RFI
- 4.3.9 Singulating/shaping
- 4.3.10 Coverlayer/Solder Mask Application
- 4.3.11 Multilayer
  - 4.3.11.1 Laminate-drill-plate
  - 4.3.11.2 Co-lamination
  - 4.3.11.3 Sequential Build-Up; BUM, etc.
  - 4.3.11.4 Other
- 4.3.12 Cleaning
- 4.3.13 Marking
- 4.3.14 Inspection & Testing
- 4.3.15 Reliability

5.0 BOARD LEVEL ASSEMBLY – PACKAGES/COMPONENTS

- 5.1 Assembly Processes
  - 5.1.1 Soldering
    - 5.1.1.1 Pb/Sn
    - 5.1.1.2 Lead-Free Solder
  - 5.1.2 Adhesive Bonding
    - 5.1.2.1 Isotropic conductive
    - 5.1.2.2 Anisotropic conductive
    - 5.1.2.3 Non-conductive
  - 5.1.3 Application of Joining Material
    - 5.1.3.1 Print/stencil
    - 5.1.3.2 Jetting
    - 5.1.3.3 As liquid; wave, pot, fountain soldering
    - 5.1.3.4 Film lamination (Z-axis)
  - 5.1.4 Mechanical for connectors & hardware
- 5.2 Placement, component
  - 5.2.1 Feed-through
  - 5.2.2 SMT
  - 5.2.3 Mixed
- 5.3 Energy Input/assembly method
  - 5.3.1 Wave soldering
  - 5.3.2 SMT reflow; IR, VP, other
  - 5.3.3 Hand – direct energy transfer
  - 5.3.4 Laser
  - 5.3.5 Direct heat; hot bar
  - 5.3.6 Other
- 5.4 Cleaning
- 5.5 Testing
- 5.6 Reliability
- 5.7 CAD
- 5.8 Modeling
- 5.9 Thermal
- 5.10 Electrical
- 5.11 Mechanical
- 5.12 Embedded Passives (can also fit 4.0)

6.0 BOARD LEVEL ASSEMBLY – BARE DIE

- 6.1 Chip-on-Board (COB)
  - 6.1.1 Die attach
  - 6.1.2 Wire bonding
  - 6.1.3 Encapsulation

- 6.2 Direct Chip Attach (DCA)
  - 6.2.1 Fluxing
  - 6.2.2 Joining
  - 6.2.3 Underfill
- 6.3 TAB (Tape Automated Bonding)
- 6.4 Other

7.0 SYSTEM LEVEL PACKAGING ("BOX" LEVEL)

- 7.1 Electrical Design/Test
- 7.2 Mechanical Design/Test
- 7.3 Thermal Design/Analysis/Management
- 7.4 EMI/RFI/Shielding
- 7.5 Connectors/Cables
- 7.6 Backplanes
- 7.7 Power
- 7.8 Opto-photonics
- 7.9 Enclosure
- 7.10 Reliability
- 7.11 Safety

8.0 SOFTWARE; CAD, FEA, etc.

9.0 ISSUES & RELATED TOPICS

- 9.1 Regulatory
  - 9.1.1 Metal restrictions; Pb, Cd, Hg, and other toxics.
  - 9.1.2 Halogen restrictions
  - 9.1.3 Take back; recycle
- 9.2 Market Phenomena
  - 9.2.1 China Effect
  - 9.2.2 Globalization job redistribution
  - 9.2.3 Other