

# WHAT IS NEEDED TO ESTABLISH FLIP CHIP AS A STANDARD SMT PROCESS

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## ABSTRACT

Flip chip (FC) is considered by many people to be the ultimate package. It deserves this reputation because it is the packaging approach that minimizes the package size and maximizes electrical performance. It is believed to be low cost because it is thought to eliminate the package. Unfortunately due to the slow, secondary processes that are

required to assemble FC, this technology can actually be quite expensive. FC will not emerge as a mainstream packaging technology unless its assembly becomes a standard SMT process. This paper discusses what process and infrastructure changes are needed for this change to occur.

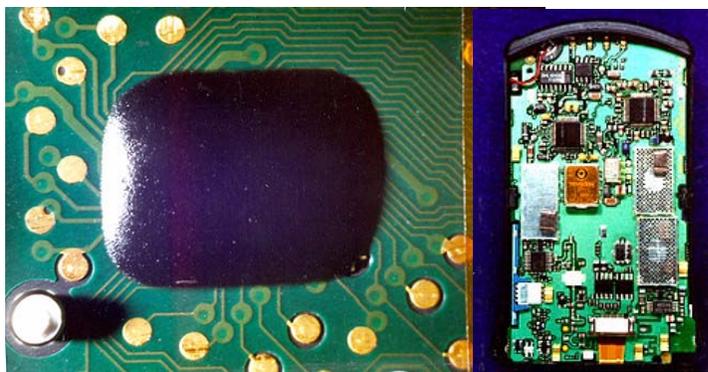
## INTRODUCTION

Flip chip (FC) may be the ultimate package. The fact that it is placed directly on the PWB eliminates one level of packaging and its inherent parasitic inductance and capacitance. Hence, because size and weight reductions are at a premium, it is a desired package. The figure below shows a typical application.

Although its small “footprint” saves on PWB “real estate,” the fact that FC (also referred to as “direct chip attach” or DCA) currently requires slow secondary assembly processes

isn’t always immediately clear. These slow secondary processes have considerable hidden costs to the final product that will continue to hinder the emergence of FC.

Cookson Electronics, working with Georgia Tech and several industrial partners, has performed an analysis to determine which equipment, materials, and processes are needed to establish FC assembly as a standard SMT process. This paper is a summary of this effort.



Motorola StarTAC Cellular Phone

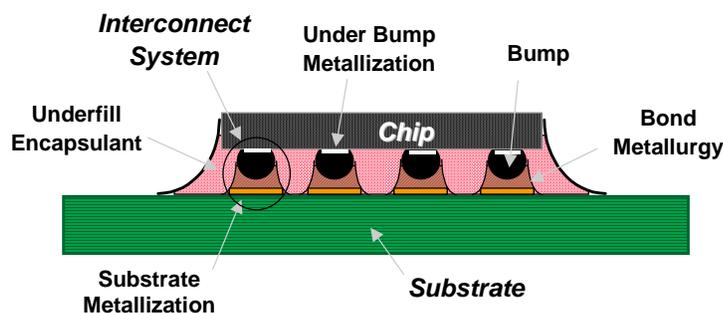


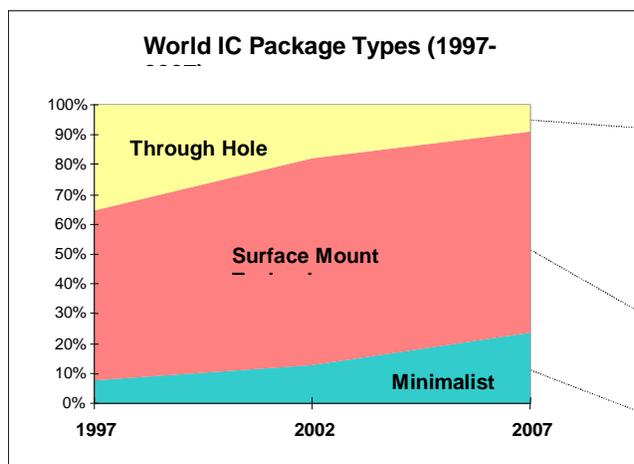
Figure 1. A typical flip chip application and a cross section of a flip chip.

**THE CALL TO ACTION**

**Flip Chip Market Projections**

Flip chip, a minimalist package, although currently representing a small portion of components assembled, is projected to grow at 35% CAGR versus all of SMT

components' more modest 9% CAGR. The following figures depict these projections.



Source: BPA

Pieces	1997	2002	2007
DIP	15.9	11.5	6.7
SIP/ZIP	3.9	3.1	2.7
PGA	0.4	0.6	0.5
Others	0.4	0.6	0.8
<b>Total</b>	<b>20.5</b>	<b>15.7</b>	<b>10.6</b>
SO	20.8	36.4	51.1
PLCC	2.3	1.4	0.6
PQFP	7.9	17.8	20.8
S M Ceramic	0.2	0.3	0.3
BGA	0.2	1.3	2.2
TAB	0.9	1.6	1.9
Other SM	1	2.1	3.4
<b>Total</b>	<b>33.3</b>	<b>60.9</b>	<b>80.2</b>
CSP	0.1	1.5	6.5
COB	3.6	6.3	13.1
Flip Chip	0.6	3.3	8.3
<b>Total</b>	<b>4.3</b>	<b>11.1</b>	<b>27.9</b>

**Total Packages (Bn)      58.18      87.64      118.76**

Figure 2. Worldwide component consumption.

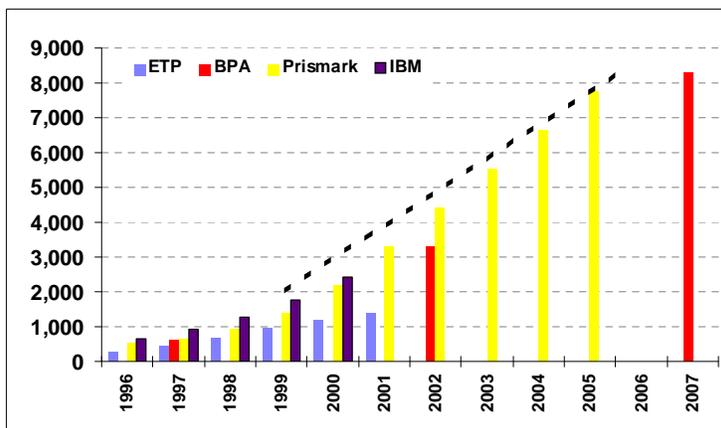


Figure 3. Flip chip use in millions of units. The CAGR is projected to be about 35%.

These numbers and growth rates do not assume the additional units that the sensor market will provide. Consequently, the many new sensor technologies that

emphasize small sizes and low weights would favor FC as an assembly process.

**The Current Flip Chip Assembly Process**

The current assembly process for FC involves slow and secondary steps to the standard SMT assembly processes.

A typical FC assembly process is depicted in the figures below.

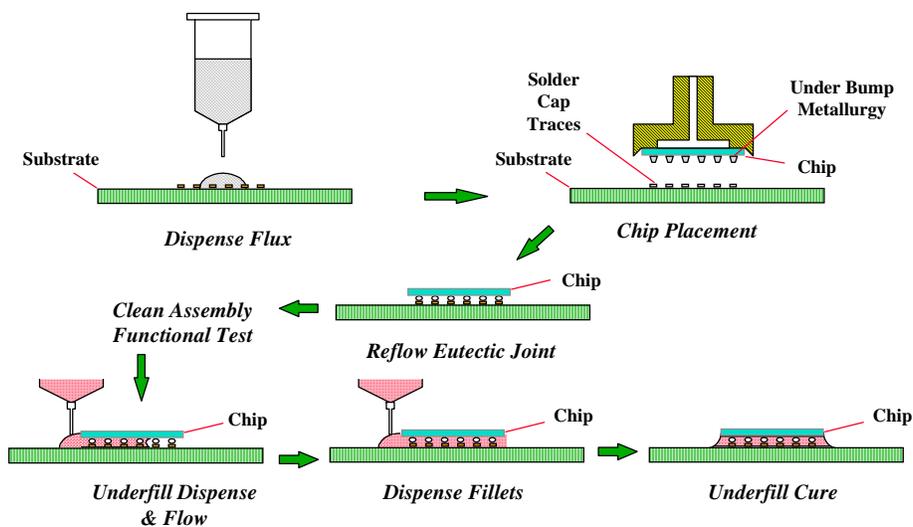


Figure 4. Flip chip assembly process schematic.

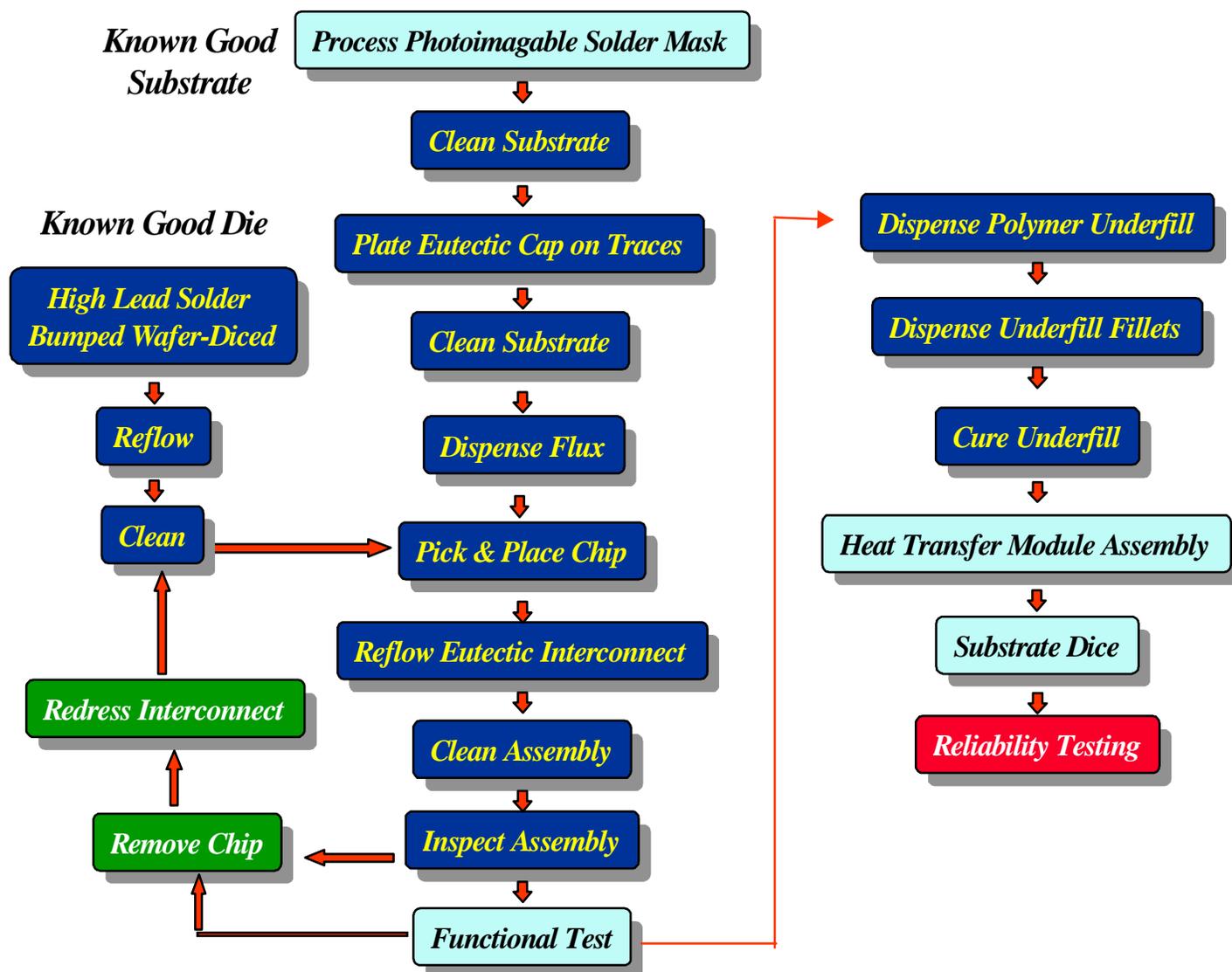


Figure 5. Typical flip chip assembly process steps.

The additional process steps required for the FC assembly process, namely, underfill dispensing and curing, have the negative effect of slowing down the assembly line cycle time. The process, however, is needed to strengthen the FC solder joints during thermal cycling. Thermal cycling causes the PWB to expand and contract more than the silicon die because the thermal coefficient of expansion of the PWB laminate material is much greater than that of the silicon of the die.

#### **The Cost Adder of Flip Chip Assembly**

Our analysis, using the cost estimating software, *SPACE*<sup>3</sup>, has indicated that the industry may lose \$1-2 billion dollars in lost production if the FC process remains a slow secondary process. It must be understood that this analysis was “generous” in that we assumed that significant

Without the underfill, the FC solder joints would quickly fail in the field due to the thermal shock of turning the unit on and off.

It has been estimated that typical FC assembly for cellular phones slows down the cycle time by more than 30%. When one considers that throughput is the critical issue in assembly today<sup>1,2</sup>, this cycle time penalty for FC is unacceptable.

incremental improvements would occur in the underfill application and curing processes. Incremental improvements, however, will never be enough. FC must become a part of the standard SMT process. Until it does, it will never be universally embraced.

In the manufacture of expensive products, the penalty is extreme. To appreciate this penalty, the following cost analysis will be performed with SPACE. Let us assume that cellular phones are being manufactured for a period of one year. The current design calls for four 100 I/O QFPs that cost \$10.00 each. These QFPs can be replaced with four FCs that

cost \$9.50 each. It would appear that choosing the FC would be a “no brainer.” The FC process, however, increases the cycle time from 25 to 32 seconds, a relatively modest 28%. We will also assume that the phones are manufactured in a “four up” PWB (i.e. there are four phones per board). Reasonable values for other variables will be assumed consistent with the assembly cost metrics in the 1996 NEMI Roadmap<sup>4</sup>. The cost input is shown in Figure 6.

Description	QFP Assembly		
Assembly Equipment(SP:\$200K, PP:\$800K, RO:\$100K, T:\$500K, BH:\$100K)	\$1,700,000.00		
Floor Space and Utilities (sq ft.) and Cost (per sq ft/month)	3682.5	\$0.83	
Components (per unit)	\$100.00		
Stencil, squeegee, lifetime (cost each, uses)	\$600.00	\$200.00	1000000
Solder Paste (\$/g), grams	\$0.1000	1	
PCB (per unit)	\$5.00		
Workers (number, rate per hour)	7	\$28.00	
Selling Price	\$130.00		
Hours per shift, Shifts per day, Days per week	10	2	6
Cycle time (seconds)	6.25		
Downtime (%)-Setup (hours per week)-Maintenance (hours per week)	8	10	12.5
Workers Supported (number, rate per hour)	26	\$42.00	
I/O	950		
Yield first pass reworkable (%)	97		
Years Equipment Depreciation	3		

Figure 6. Input data for SPACE software to calculate QFP assembly cost and profit. Cycle time is 6.25 seconds per phone because of “four up” assembly design.

Input for the FC assembly case requires 1) an increase of 7 seconds in unit cycle time (28 seconds divided by 4), 2) an increase in assembly equipment cost from \$1.7 million to \$2.0 million, 3) a 20% increase in floor space cost, 4) an increase of \$0.50 each PWB (\$0.125 per phone) in consumable

materials (for the underfill and supporting materials, this increase is inputted with the solder paste), and 5) an increase of two line workers and one support worker. On the positive side, the component cost is reduced by \$1.00.

	A	B	C	D	E
20	<b>Cost</b>		<b>\$ Per Board</b>	<b>%</b>	<b>Total \$</b>
21	<b>Components</b>		\$ 100.00	91.938	\$ 263,267,700.00
22	<b>Labor</b>		\$ 3.05	2.807	\$ 8,037,120.00
23	<b>PCB</b>		\$ 5.00	4.597	\$ 13,163,385.00
24	<b>Consumables</b>		\$ 0.10	0.093	\$ 265,373.84
25	<b>Machine Cost</b>		\$ 0.29	0.262	\$ 750,719.72
26	<b>Rework</b>		\$ 0.32	0.290	\$ 829,293.26
27	<b>Floorspace, Utilities</b>		\$ 0.02	0.014	\$ 39,842.25
28	<b>Total</b>		\$ 108.77	100.000	\$ 286,313,591.81

Figure 7. Cost output from SPACE for the QFP assembly.

The cost analysis from SPACE is in Figure 7. It is interesting to note the small relative unit cost of assembly equipment, consumables, and floorspace/utilities. A

comparison of the unit cost, profit, and number of phones produced in the two processes is given in Figure 8.

### Run Comparison

Descriptor	Unit Cost	Unit Profit	# Units	Total Profit
QFP Assembly	\$108.77	\$21.23	2,632,677	\$55,894,574.85
FC Assembly	\$108.99	\$21.01	2,056,779	\$43,210,813.26

Figure 8. A cost comparison of the QFP and FC assembly processes.

Clearly, the unit cost difference is not great, but the total profit difference is stunning. The increased cycle time for FC results in significantly fewer units being produced. In a

facility with eight such lines, the total profit lost in one year would be over \$100 million.

### FLUX/UNDERFILL: A FIRST SOLUTION

A proposed process solution to establish FC as a standard SMT process is called "Flux/Underfill." This process uses a material that can act as the flux for the FC reflow and then can

cure to be the underfill. Schematics of this process are in the figures below.

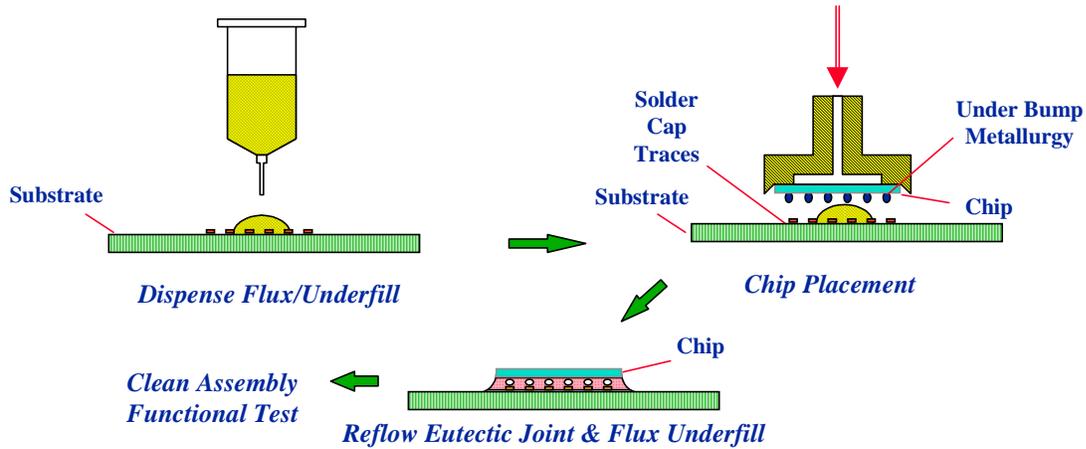


Figure 9. Low-cost flip chip assembly with a flux underfill.

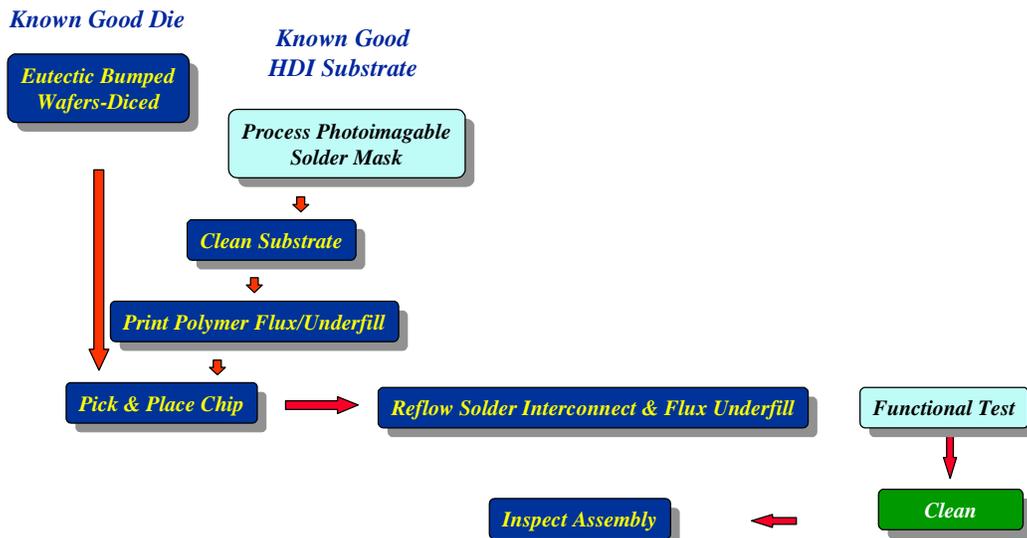


Figure 10. The flux/underfill process steps.

Note that the flux/underfill process eliminates the two cycle time courses of dispensing and curing the underfill after the die is reflowed. Preliminary work has been performed on this process at Georgia Tech. The team, under the direction of Professors Dan Baldwin and C. P. Wong, has developed a material (and process) that appears to be able to assemble FC die that are up to 2 cm on a side. We consider this process to be a prime contender to establish FC as a standard SMT process.

Another process that could allow FC to be a standard SMT process is often referred to as a wafer level underfill. In this process, the underfill is applied to the wafer before it is diced.

After the dicing process, the die can be placed and reflowed as shown in Figure 11. The process technology for this approach does not appear to be as advanced as the flux/underfill process. Hence, it will probably be a follow-on solution for FC as a standard SMT process.

Figure 12 is a schematic of various manufacturing processes to produce wafer scale FC. In a sense, the resulting product could be considered a chip scale package (CSP). One advantage of wafer scale FC is that it does not require the fillet of underfill that the normal FC process does. This fillet occupies PWB "real estate" which adds cost.

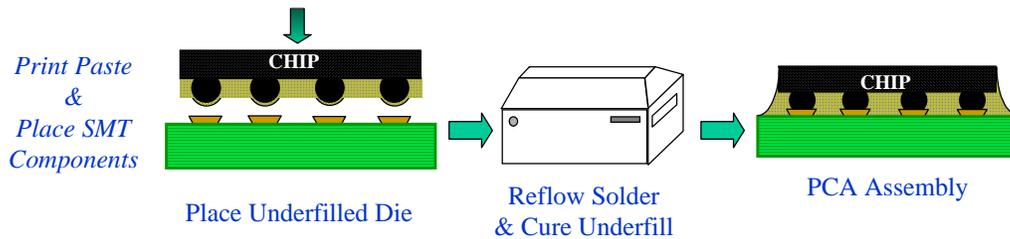


Figure 11. Wafer level FC requires the same assembly process as a standard SMT process.

## WAFER-LEVEL FLUX/UNDERFILL

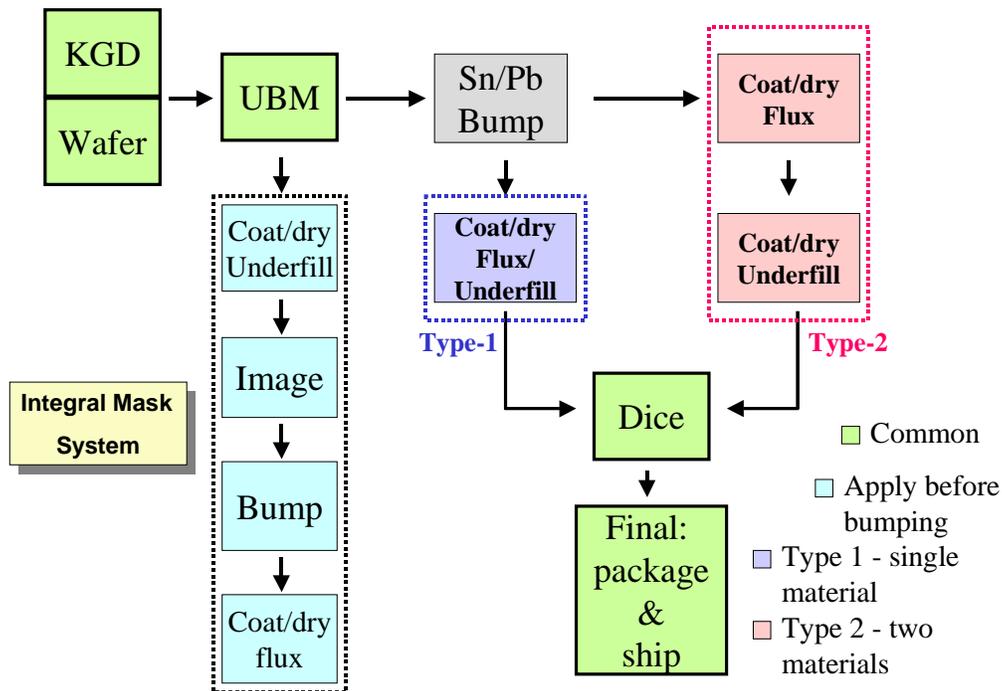


Figure 12. Various process steps in manufacturing wafer scale flip chip underfill.

## ISSUES BEYOND ASSEMBLY: THE INFRASTRUCTURE

Although it may seem that success of the flux/underfill program would solve the major issues impeding the rapid implementation of FC, this belief would miss a major point. An equal challenge to proliferation of FC is what could be

broadly stated as infrastructure issues. These issues can be categorized as pre- or post-assembly. The following table lists them, designating wafer level-only issues by (WL):

Issue Number	Pre-Assembly	Post Assembly
1.	Availability of known good die that are "bumped"	Reliability testing and test data
2.	Availability of organic substrates at a reasonable cost	Dicing of wafer (WL)
3.	Redistribution on wafer (WL)	Packaging of diced die (WL)
4.	Under Bump Metallization (UBM) on wafer (WL)	
5.	Backgrinding on wafer (WL)	

Table 1. Infrastructure issues impeding the rapid implementation of flip chip.

The availability of known good die and organic substrates to support FC are considered by many to be the key issues holding back FC implementation. Currently it is impossible to find one vendor that can, in house, take a wafer, bump the die, singulate the die by sawing and grinding, and then place it in a wafer pack or another type of "presentation" packaging for the pick and place machine. In addition, the current cost of performing these processes is prohibitive. The substrate challenges are no less discouraging. There are few vendors in

the US that can deliver, in quantity, low-cost substrates to support FC. The technologies needed to manufacture the fine lines, high density via and pad concentrations are currently mostly in Japan.

Any proposed process technology to establish FC as a standard SMT process must be tested thoroughly for the reliability of the resulting product. The type of testing needed to establish reliability and the required test equipment is not commonly within the expertise of a typical assembler.

## CONCLUSION

The advantage to be gained by developing the technologies to establish Flip Chip as a standard SMT process is a cost savings to the industry of \$1-2 billion in the year 2001. This estimate may be conservative as establishing such a process may allow FC to eat into the market of other minimalist packages such as chip scale and chip on board packages.

Our analysis suggests that a process such as the flux underfill process mentioned in this paper could fill this need. There are, however, also significant infrastructure needs in the supply of known good die and low-cost substrates that must be developed to support large-scale adaptation of FC.

Cookson Electronics and Georgia Tech plan to work with several partners to address these needs in the near future.

## REFERENCES

1. Lasky, R.C. and Baldwin, D.F. "Throughout the Critical Cost Variable in DCA Assembly," Proceedings of the SMTA 3<sup>rd</sup> National Symposium, Research Triangle Park, NC, pp. 1-7, 1996.
2. Lasky, R.C. and Baldwin, D.F., "Critical Cost Analysis of the Flip Chip Assembly Process," Presented at the 2<sup>nd</sup> *IMAPS Advanced Technology Workshop on Low Cost Flip Chip Technology*, Braselton, GA, March 13-15, 1998.
3. *SPACE* is a proprietary software program developed by Ron Lasky of Cookson Electronics. *CostCoach*<sup>TM</sup> is a commercially available similar product. It is marketed by ITM. Email: [theitmtteam@aol.com](mailto:theitmtteam@aol.com).
4. 1996 National Electronics Technology Roadmap, NEMI, Herndon, VA, 1996.

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