The Great Underfill Race

By Dr. Ken Gilleo – Ken@ET-Trends.com

David Blumel

Abstract

Most Flip Chip assemblies require underfill to bestow reliability that would otherwise be ravished by stress due to thermomechanical mismatch between die and substrate. While underfill can be viewed as "polymer magic" and the key to modern Flip Chip success, many see it as the process "bottleneck" that must be eliminated in the future. Both views are accurate. A substantial amount of R&D is being focused on making underfill more user-friendly. Electronic materials suppliers, various consortia, government labs and university researchers are working diligently to *shatter the bottleneck* and fully enable Flip Chip - the final destination for micropackaging. This paper will describe these efforts and provide a status report on state-of-the-art underfill technologies. We will also examine new processing strategies.

Today, three distinctly different underfill systems vie for victory: capillary, pre-dispense and solid film. The incumbent capillary flow underfill manufacturers attempt to win by offering snap flow/snap cure materials and new features. Can the new 5-minute cure underfills deliver enough throughput and performance? Will the so-called "No Flow", or pre-dispense liquids, win by eliminating flux even though dispensing equipment is still required? Which systems are REWORKABLE and how important is this feature?

Perhaps the ultimate solution is solid underfill, but can the polymer chemists meet such a challenge wrought with paradox? How and where should solid underfills be applied and processed? Learn the status of the most unusual approach - Reworkable Wafer-Level Flux-Underfill. Success at wafer-level can have a profound affect on Flip Chip by eliminating all steps and equipment now associated with the underfill process. We will try to determine if wafer-level underfill can deliver on the promise of making *Flip Chip the Ultimate CSP*!

Key words: Flip Chip, capillary flow, Chip Scale Package, flux, polymerization, reworkable, thermoplastic, thermoset, underfill, wafer-level

Introduction

The *Packaging Revolution* of the 1990's continues to introduce the most significant and rapid changes yet seen in the electronics industry. While the shift from feed-through component assembly to surface mount took about 80 years, the transition from perimeter leads to area array is happening in less than a decade. The relentless drive for *smaller-faster-thriftier* electronics, propelled primarily by portability, now thrusts the industry into chip-scale and chip-size packaging. The ultimate destination appears to be "packageless" components as embodied by the Flip Chip.

The 1st generation ceramic-based Flip Chip technology has had an enviable record of success in main frame computers and automotive controllers. Reliability and performance have been nothing short of incredible. IBM claims to have once passed 60,000 thermal cycles in what may have also been a record of test perseverance. The computer and automotive industries continue to rely on Flip Chips assembled to low expansion ceramic substrate.

Later, other industries sought to bring the tantalizing Flip Chip down to the world of consumer electronics where our demands for portability, power and performance outstripped the capability of the available packaging technologies. Flip Chip certainly holds the record for speed and performance. The missing factor was "thriftier", but all that this required was a seemly small, yet profound, change in technology. Thrift for Flip Chip meant a paradigm shift in the primary substrate. The simple answer was to move to organic substrate and this is what 2nd generation Flip Chip is mostly about. But the "simple" conversion from low expansion inorganic to high CTE (Coefficient of Thermal Expansion) organic PCB would appear to require a suspension of the *laws of science*. What happens if unyielding low CTE silicon is joined to high expansion epoxy laminate by tiny solder bumps? Nothing, of course – until the tem-

perature is changed. Then, damaging stress is produced. Unfortunately, most electronic devices experience thermal cycling during power up/down and often during operation. The thermal cycling inevitably generates a destructive stress factor that fractures the joints in short order as shown in Figure 1.

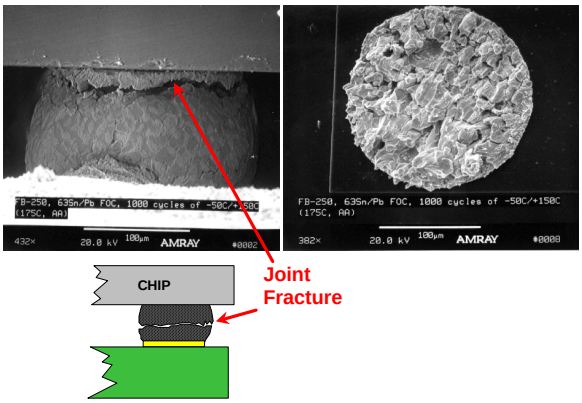

Figure 1 – Fractured Joint
Courtesy of Flip Chip Technologies, Inc.

Most of you know how this problem was solved. The *almost-too-simple* solution was to add underfill between the chip and substrate. Underfill is simply an adhesive that mechanically couples the chip-to-substrate to restrain much of the differential movement between the two interfaces. The interconnecting joints are therefore protected and preserved. It is important to keep in mind that only the X-Y plane expansion is coupled. The Z-axis expansion is free to expand and it must accommodate the properties of the joints. Most now concur that the CTE of the underfill should approximately match that of the joints; ~ 25ppm/^{o}C for eutectic solder.

Underfill products are now available that deliver on the promise of providing the reliability required for 2nd generation Flip Chip on organic platforms. Millions of Flip Chips are now being assembled on FR4 and BT laminate for such a wide range of products as cellular phones, pagers, disk drives, memory modules and much more. These 2nd generation Flip Chip assemblies are literally in the hands of consumers and performance continues to meet or exceed expectations. Now that quality and performance are somewhat assured, the focus is shifting to manufacturing productivity.

The newest state-of-the-art underfills have been revved up to provide “snap flow” and “snap cure” with a color change option to signal completion of cure. It would seem that 2nd generation Flip Chip is one of the great success stories of the Packaging Revolution and perhaps the underfill formulators should retire or retrain. Wrong! The present capillary underfill is really only the first phase of this technology and we have a way to go for truly optimum underfill. First, let’s categorize the basic types of underfills.

Classes of Underfill

Capillary Flow

Flip Chips are typically assembled to the substrate, tested and then underfilled, although some line configurations may test last. The very nature of the fill process requires that the underfill be in a liquid state, at least during the flow step. While one could perhaps use gravity or fluid pressure to flow the underfill into the gap, surface tension, or capillary flow is used. Capillary flow utilizes the basic principal of surface chemistry. Intramolecular attraction must exceed intermolecular forces. The underfill resin molecules (continuous phase) must be more strongly attracted to the chip and substrate surfaces than to one another so that an advancing contact angle is achieved. An advancing contact angle means that the liquid is wetting the surface and is advancing forward – the liquid molecules are being attracted to the surface substrate molecules (or atoms). This is accomplished by insuring that the surface tension of the underfill is lower than the surface energy of the solid surfaces to be wet. Addition of wetting agents generally produces the desired low surface tension. The energy of wetting is the “engine” that pulls the underfill along the gap while the resistance of viscosity acts to retard the flow.

Although early capillary flow underfills had slow flow rates because of higher viscosity resins and unoptimized filler morphology, today’s materials flow rapidly with rates of 25 mm/minute, or higher, provided that the substrate is heated (~80^{o}C) to reduce viscosity. We appear to be approaching the limit of accelerated flow rate. Resin viscosity can’t be made much lower, surface tension cannot be dropped much more and filler particles can’t be made much smoother. Still, many assemblers, not to mention CSP competitors, continue to shout, “Bottleneck, bottleneck”. Are they right? Yes! The best underfills add a time penalty and increase the cost. But if the capillary flow underfills are "maxed" out, what can we do?

Figure 2 displays fast flow while Figure 3 shows color-change-on-cure to exemplify state-of-the-art capillary flow underfill progress. The color change underfills give the factory line an instant warning if something is amiss. The high contrast change occurs during the last 5% of cure providing an accurate indicator for adequate polymerization.

Figure 2 – Snap Flow

Pre-dispense ("No Flow") Underfills

Scientist and technologists have spent several years working on underfills that can be applied to the substrate before the Flip Chip is assembled. We prefer the term, *pre-applied* or *dispense first*, underfills, instead of the more rhythmical, but less accurate, "No Flow". Be assured that the "no flows" do flow. The pre-applied type of underfill product must also provide the flux activity required for the solder bumps to form joints with the pads on the substrate. Most of today's underfills are based on anhydride hardeners that afford some level of flux action anyway. Anhydrides hydrolyze to carboxylic acids that are common ingredients for flux.

The first challenge for the pre-applied underfills was to slow down the polymerization rate. Standard underfills are designed to cure at about 150°C. When the temperature is boosted to 215°C to 225°C, used for solder reflow, polymerization is greatly accelerated. Chemical reactions typically double in rate for every 10 °C increase in temperature. The acceleration at 220°C can cause a standard underfill to harden well before solder has properly melted and formed joints. Even if catalysts are completely removed, leaving only resin and hardener, the rate may still be too fast. The pre-applied underfills really require a total reformulation.

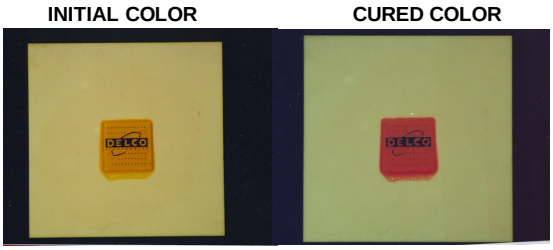

Figure 3 – Color Change

Several companies have explored the pre-applied underfills and a few commercial products have become available. Georgia Tech has done substantial work in this area and reported on it extensively[1-5]. Let's now look at how the pre-applied process is used and at the advantages and limitations. The process begins with dispensing the underfill onto the flip chip-bonding site of the circuit or chip carrier. The work at Georgia Tech has shown that both the amount of material dispensed and the patterns are very critical. Too much underfill will cause the chip to "float" and form incomplete solder joints or none at all. But, too little underfill will cause voids under the die and incomplete filleting. The underfill must be symmetrically dispensed or the chip will tend to skew or move off center. But even if the correct volume and pattern of underfill is dispensed, the remaining steps of the process must be carefully controlled for acceptable results.

The Flip Chip must be placed in a way that assists in displacing air so that voids will be minimized. There is a tendency to trap air as the bumped chip is placed into the underfill unlike capillary underfills where the flow front displaces air. One of the more advanced techniques, called compression flow[1], is shown in Figure 4. The downward movement causes the "no flow" underfill to flow outward to the edges of the chip. The compressed underfill, with a generally symmetrical outward flow pattern, helps displace air and may be the preferred method. Figure 5 contrasts capillary flow and compression flow.

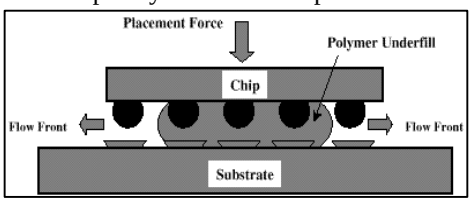

Figure 4 - Georgia Tech – ref. 1

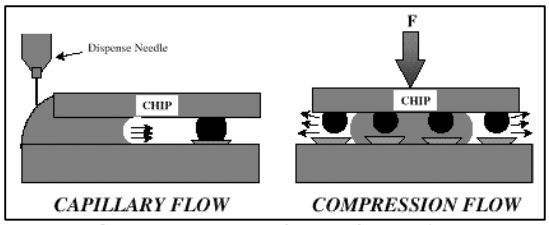

Figure 5 - Georgia Tech – ref. 1

Some considerations for dispense-first underfills are:

- Smaller bump size reduces voiding.
- Larger pitch reduces voiding.
- Substrate temperature is critical for each underfill material to reduce voiding.
- Too low a viscosity allows gravity flow that increases voids.
- Low deposition height increases voids and causes starvation.
- High viscosity allows compression flow to dominate and is preferred.

Once the underfill flow out is complete, the curing strategy must be considered. Should the cure chemistry be designed for completion by the solder reflow heat exposure? The resin/hardener reactivity can be adjusted so that the short exposure to approximately 220°C is all that is required. However, the complete curing of a thermosetting underfill precludes rework. The opportunity for pre-testing is lost since soldering and underfill curing occur concurrently.

Another strategy is to reduce the reactivity so that reflow-soldering conditions gel the underfill. Now the chip can be reworked. However, the assembly must be post-baked after testing to fully cure the underfill. The delayed polymerization chemistry used to prevent full curing during soldering now works against productivity. A 1-hour post bake is typically needed for the "reworkable" "no flow" underfills according to commercial literature. Since capillary flow systems can underfill in seconds and cure in minutes, the productivity gain for the reworkable product appears to have evaporated. We need to keep in mind that all capillary flow underfills can allow reworking provided that testing is done after reflow soldering, but before underfilling. So if capillary flow is a bottleneck and "no flow" is perhaps an impaired solution, what is left? How about *solid* underfill?

Solid Underfills

Conventional wisdom suggests that underfills should be liquids, or at least pastes, since they need to flow. But solid "underfills" have been used commercially for many years. Why haven't we heard about it then? The simple reason is that these materials have not been viewed as underfills. But if we examine Anisotropic Conductive Adhesives (ACA) more closely, we will find a solid underfill. ACAs, commonly called Z-axis adhesives, have been used for Flip Chip assembly for more than a decade. We can view ACA film for Flip Chip assembly as solid underfill containing a small percentage of conductive particles. Figure 6 shows a diagram of such an assembly. Some may argue that the dielectric film is really an adhesive and that is correct. However, underfill should be viewed as adhesive film that mechanically joins the Flip Chip to substrate. Underfill laminates the Flip Chip to the substrate and this adhesive mechanical coupling reduces the differential movement that would destroy the Flip Chip joints. The ACA film and the underfill really do have a lot in common. Now let's get back to underfills.

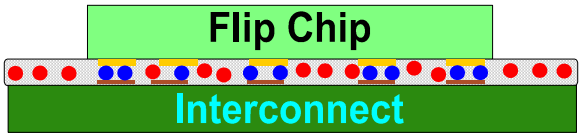

Figure 6 - ACA

What properties are required for a solid underfill? The material, after Flip Chip assembly, should have properties similar to the common capillary flow products after they are cured. The Coefficient of Thermal Expansion (CTE) should be reasonably low (<35 ppm/°C) and the various thermal properties, especially glass transition temperature (Tg) should be adequately high (Tg >125°C). These properties are not difficult to achieve. The material would also need to bond strongly to chip and substrate in film form. ACA films have long demonstrated the viability of bonding using heat and pressure, so this should not be a serious problem. But are there any solid underfills on the market yet?

One company recently introduced a solid film referred to as resin sheet underfill[6]. Here's how it works. The resin sheet is first laminated to the circuit board using a custom machine. The Flip Chip assembly step, as is the case with ACA films, requires force to be applied so that the chip bumps will displace the resin and make contact with the circuit pads. Once again, special Flip Chip bonder must now be used. While the resin film underfill certainly demonstrates that solid underfill is possible, the benefits provided appear to be somewhat offset by requiring a laminator

and a customer bonder. But is there another means of deploying a solid underfill for better processing logistics?

Wafer-Level Solid Underfills

The most reasonable location for solid underfill is on the bottom, or bumped side, of the chip. A Flip Chip that already has the necessary underfill begins to take on characteristics of a Chip Scale Package. The solid underfill, of course, must also have flux characteristics, but the "no flow" underfills and resin sheet have demonstrated that this can be done. There is one more important property to be considered for the wafer-level solid film underfill. The product should be reworkable and retain that characteristic after assembly and any post processing steps. A readily reworkable underfill would transform the Flip Chip into a true package. Most packaging specialists insist that a package must be removable and preferably reworkable to qualify as a genuine electronic package. Chip Scale Packages (CSP) have had the advantage of reworkability along with other features, but at a cost penalty. The addition of a solid reworkable flux/underfill to the FC moves it to the CSP domain. There are very significant ramifications for this type of package.

There are at least two approaches for constructing a *ready-to-assemble* Flip Chip Package. A single material, with combined flex and underfill properties, can be used. But is it practical to combine flux and underfill into one material? Although the previously discussed liquid "no flow" underfills have already demonstrated that flux and underfill properties can be merged, adding the reworkability requirement increases our challenge although such a system is still feasible. A two-layer system, however, is easier to formulate although more complicated to apply to the chip. But, let's compare the two approaches.

A Two-Layer Flux & Underfill System

The two-layer concept involves applying a reworkable underfill to the bottom of the bumped chip at wafer-level and flux to the proximity of the bumps. The underfill can be a thermoplastic that introduces the reworkability property. The material could be applied as a liquid or paste from solvent by spin coating, stencil printing, spraying or any number of methods used for liquid dispensing. The material could also be applied as a film by lamination. Still another possibility is to apply a powder and melt it into a film (powder coating). A variety of thermoplastics are available that can be considered. Thermoplastic films and pastes are now used for reworkable die attach applications[7]. Some of these die attach products are applied as pastes to the back of wafers followed by drying. These systems could be modified with the appropriate silica fillers to become underfills coated onto the active side of the die.

The next step would be to apply the flux to bumps. Again, a number of methods are available, including simply dipping the wafer into a thin layer of flux so that only the bumps are coated. Today, flux is applied to the bumps of single flip chips by such a dipping method using a fluxing drum available from many assembly machine vendors. Drying would harden the flux, once applied. Figure 7 shows the final result for the two-layer process.

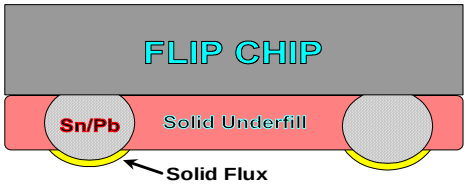

Figure 7 – Two-Layer Flux/Underfill

One-Layer Flux/Underfill

A single-layer reworkable flux-underfill solid presents several non-trivial challenges but none of the required properties are mutually exclusive. The material would needed to an underfill and therefore have a lower CTE, a high Tg and good adhesive characteristics. Flux properties are only needed during solder attachment and many chemistries are available from the no clean flux area. The fully processed product should be reworkable at about 180°C. Our own strategy has been to start with a solid epoxy-based flux and design a polymerization chemistry that produces linear rather than the more typical cross-linked polymerization. The linear polymer, that can have a low level of cross-links, will soften at elevated temperatures to provide reworkability. Our work, to date, has shown that good flux activity can be achieved with a solid system and that linear polymerization is practical in an epoxy resin phase. The solid flux/underfill was applied to a single chip and dried before assembly. The substrate for these preliminary tests was copper laminate that was allowed to first oxidize. Transparent 12.5 mm square chips with eutectic solder bumps were used for easy observation.

The ultimate wafer-level flux/underfill should not require force applied to the chip during assembly although a product that required a Flip Chip bonder would still have high value. Our present expe-

rimental system does not appear to require downward force since the solid film initially melts at 80°C and quickly wets the substrate. Polymerization proceeds with gelling occurring just after solder joint formation. Our 220°C exposure triggered the desired polymerization. The final system remained reworkable as expected. However, the linear polymerization did not produce a high enough molecular weight and the typical softening point was only about 100°C instead of the desired 180°C. We hope to have more results by conference time.

Conclusions

The state-of-the-art underfills flow rapidly and cure in only 5 minutes. However, the time and equipment burden required for underfilling limits Flip Chip technology. Solid flux/underfill as an integral part of the Flip Chip is the logical path for optimizing and fully enabling this technology. Reworkability is an important property that will transform the Flip Chip into a true Chip Scale Package to take advantage of the SMD infrastructure. Our initial work has gone a long way in demonstrating the feasibility of solid underfill/flux. Continued work in this area is likely to produce the desired product that will have major ramifications for the packaging industry.

Future Work

The significant remaining obstacle is the low softening point. Our efforts, directed toward boosting this property, include starting with higher molecular weight linear epoxies, introducing cross-linking agents at a low level and adding a post bake if the other approaches are insufficient. The second phase of work will focus on wafer-coating methods and will include stenciling, spin coating and spraying in partnership with MPM Corporation and Specialty Coatings Systems.

Acknowledgements

Professors C.P. Wong and D. Baldwin, of Georgia Tech, provided helpful discussions. R. Godin and A. Johnson, of MPM Corp., advised us on stenciling and printing methods for wafers. A. Qureshi, of Specialty Coatings, Systems provided initial testing and consulting on the use of spray and spin coating of bumped wafers. D. Patterson and R. Benson, of Flip Chip technologies, advised us on several areas of Flip Chip production and the issues associated with processing wafers coated with solid films.

References

1. Pascarella, N. and Baldwin, D., “Compression Flow Modeling of Underfill Encapsulants for Low Cost Flip Chip Assembly”, 48th ECTC, Seattle, WA, May 1998, pp. 463-470.

2. Baldwin, D. and Pascarella, N., “Manufacturability of Underfill Processing for Low Cost Flip Chip”, ASME International Congress and Expo., Dallas, TX, November 1997.

3. Han, S., Wang, K., and Cho, S., “Experimental and Analytical Study on the Flow of Encapsulant During Underfill Encapsulation of Flip-Chips”, Proc 46th Electronic Components and Technology Conf., Orlando, FL, May 1996, pp. 327-334.

4. Pascarella, N. and Baldwin, D., “Advanced Encapsulation Processing for Low Cost Electronics Assembly – A Cost Analysis”, 3rd International Symposium and Exhibition On Advanced Packaging Materials, Processes, Properties, And Interfaces, Braselton, GA, March 1997, pp. 50-53.

5. Pascarella, N. and Baldwin, D., “Advanced Encapsulation Processing for Low Cost Electronics Assembly – A Cost Analysis”, Advances in Electronic Packaging – ASME INTERpack ’97, Vol. 19-1, June 1997, pp. 359-363.

6. Ito, S., et al, “A Novel Flip Chip Technology Using Non-Conductive Resin Sheet”, 48th Electronic Components & Technology Conference, Seattle, WA, May 1998, pp. 1047-1051.

7. Gilleo, K. et al, "Thermoplastic Die Attach Adhesive for Today's Packaging Challenges", Electronic Packaging & Production, pp. 109-112, Feb. 1994.