"Flip Chip vs. CSP – Still a Close Race"

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The classic *FC Vs CSP* race, driven by our never-ending quest for performance & portability, has lasted over thirty years with no clear victor. That's right, these two micro-package contenders have been around since the 1960's. We've all heard how IBM invented the flip chip, but the creation of a CSP at AT&T about the same time hasn't been noted. AT&T's Allentown, PA facility was faced with the problem of boosting density beyond the limits of that day. The simple solution was to add short gold beam leads around the chip's perimeter encapsulating the junctions with silicone polymer.

Here we are in the 21st century faced with the same age-old density dilemma. How can we minimizing package size while optimizing performance in the most cost-effective manner? And let's be candid. Cost is often the decisive factor. Flip chips and Chip Scale Packages offer similar attributes so cost may decide the winner. Neither technology offers a decisive advantage nor has a strong hold in any market. Granted, FC has design wins for CPUs at Intel, AMD and IBM, but performance memory, like RAMBUS, has embraced CSP. But this could flip flop. FC and CSP are both enjoying accelerating growth, but will either dominate in the next few years?

Some call the flip chip the ultimate package since nothing can be smaller, nor boast more I/Os (IBM claims +10,000) and nothing has better electrical performance. So why even bother with a CSP? Well, what about recurring die shrinks and standardization whose lack exacerbates chaos? And yes, what about rework? And the "U' word – UNDERFILL! Everyone hates it – the bottleneck that could sideline the ultimate *packageless* package! OK, these are good arguments for CSPs.

Is there a problem in measuring the candidates? As both technologies evolve, the difference blurs making the distinction sometimes arbitrary. A look at market projections shows a close race for many more years and discrepancies among pundits could be in their definitions. Is Sandia's bumped chip rerouting system a modified FC or is it a CSP? When a flip chip BGA meets the size criteria, is it a CSP? And the Sony HandyCam with FCs, CSPs and/or FC-CSPs allowed both factions to claim victory. So maybe we do need a re-definition instead of more names like "flipped CSP".

Let's take a final look at cost so tightly linked to productivity. CSP has moved to wafer-level manufacturing and this may tilt the balance. But FC has been a wafer-level process for decades and new low cost bumping will improve economics. Still close, but what about underfill - the Achilles heel of FCs? Can we eliminate it? Fix it? Maybe to both! We've been hearing that a major breakthrough is on the horizon, but its iffy. The answer to underfill "IF" may be "XUF". Specifically, NUF, WUF and MUF. We've seen the commercialization of "No Flow" underfill (NUF) that removes several steps. And right behind this could be Wafer-Level (WUF) solid *built-in* flux-underfill promising *ready-to-bond* FCs. Or is the answer new molded underfill (MUF)? Stay tuned while noting that our *person-of-the-century* Albert Einstein suggests, "Everything should be made as simple as possible, but not simpler".