Chip Packaging 2.0 Provides Benefits to Board Designers

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Experts skilled in the art of PC board design have probably experienced the "last pin" debacle. You're wrapping up a complex design after months on the project, giving it your best effort of hands-on experience and intuition. You've employed a robust autorouter to assist along the way. Lo and behold, your circuit comes to a halt due to an *orphan pin* to route. Hence begins the hand wringing. Do you add another layer? Add blind, or buried vias? Spend countless hours retracing your steps. You see a wall, but there may be a *doorway for opportunity*.

What if you had a new tool in your tool-kit that could solve the problem? What if you were suddenly empowered to remap the chip pinouts without changing the performance of the silicon? Is this fantasy and science fiction? Have the authors gone mad?

Board designers have an unending need to develop optimal circuit board designs. However, board designers are constrained from fully optimizing boards in what is called the current "Chip Packaging 1.0" design and manufacturing paradigm. Chip Packaging 1.0 is what the industry fundamentally practices today; wherein, the chip design team defines the package and pinouts as documented in the chipmaker's datasheets. Chip designers optimize the *silicon-to-package* I/O to suit their needs, leaving it to others to figure out how to layout the *package-to-board* connections.

This, in the current Chip Packaging 1.0 environment, the board design team has no ability to change any aspect of the IC package or to re-map the pinout. Unfortunately, no viable communication channel yet exists between the chip design team and the board designer. Packaged legacy chips are simply tossed over-the-wall to board designers who are highly constrained in today's Chip Packaging 1.0 world (Figure 1). Presently, chipmakers have almost no motivation in talking with board designers about improving legacy chip packing. Board designers thus have one hand tied behind their back from the very beginning of the board design cycle.

Figure 1. Chip design team defines the package pinout without collaboration with the board design team.

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There is a clear need to change. Rather than continue failed attempts at jumping over the wall, there is an opportunity for a call to action that provides board designers a pathway to simply walk around it. In the proposed new "**Chip Packaging 2.0**" era, an environment is chartered wherein board designers are fully empowered to re-map package pinouts of legacy chips using without altering the performance of the silicon. Imagine a paradigm shift in which board designers routinely use EDA software to freely iterate legacy IC packaging pinouts while simultaneously optimizing the board's routing (Figure 2). Such "User Definable Pinout" legacy chip packaging is referred to as **UDPo**.
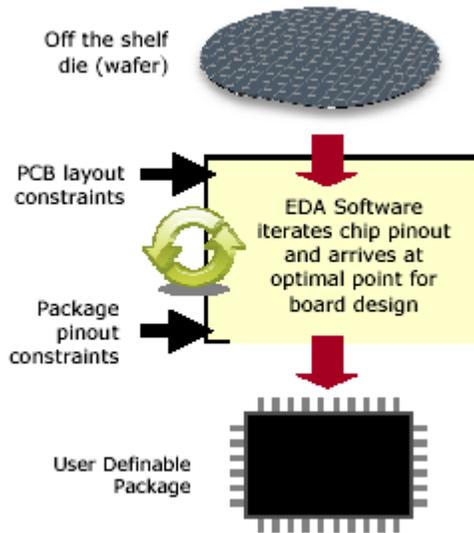

Figure 2. EDA software iterate chip UDPo – User Definable Pinout package while optimizing board design

Board designers follow familiar rules for laying out the circuit board's initial design in the Chip Packaging 2.0 environment. As is usually the case, the board designer begins by making a series of tradeoffs between electrical, thermal and mechanical needs. Once component locations are established, the circuit schematic is loaded and autorouting of the board commences. The iteration begins by benchmarking the initials results achieved with "standard pinout" packages. Next, the EDA chip pinout optimization software begins the iteration process. Pairs of pinouts on selected IC packages are iterated while board routing performance is observed. During the iterative process, improvements are observed as copper routing is shortened, board size is reduced and/or fewer inner layers are required. Typically, the pinout of only one legacy chip at a time is iterated and optimized, then cycled to the next legacy chip until the total circuit board is optimized to the satisfaction of the board designer. Board designers are free to pick and choose which legacy chip packages to iterate. Once the board is totally optimized, the EDA software will output a chip-bonding schedule (net list), which is sent by Internet (or conventional means) and inputted into IC wire-bonding machines during the legacy die/packaging assembly process.

Let's walk through a very simple circuit design. For purposes of discussion, figure 3 illustrates the non-optimized "before" board design. U1 and U2 are *off the shelf* 8 pin SOIC packages. The copper routing on the PC board from U1 pin 4 to U2 pin 7 crosses the copper routing from U1 pin 5 to U2 pin 8. To prevent short circuits, board designers would typically add a layer with plated vias to complete the design.
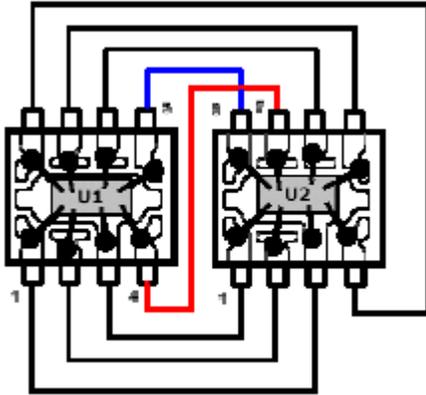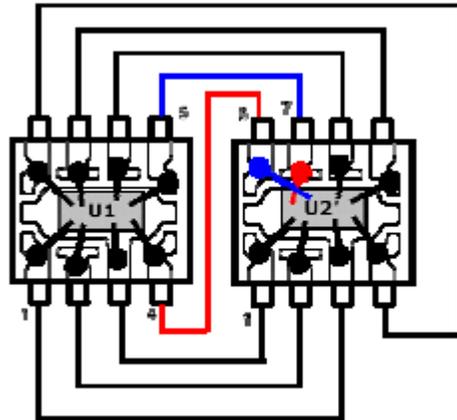

Figure 3. "Before" non-optimal board design

Figure 4. "After" optimized board design

The board designer uses EDA optimization software to optimize the board design as shown in Figure 4. After completing the chip pinout iteration process, the EDA software determines that a pair of bonding wires inside U2' should be remapped. The re-mapped U2' results in the crossing of bonding wires from die pad 7 to lead frame pin 8 and from die pad 8 to lead frame pin 7. Magically, the board design is optimized by the EDA software with shorter copper routing, fewer layers and less vias. The EDA software outputs a bonding schedule (net list), and the data is presented to IC fabricator (subcon) to assemble the legacy die (or wafer) in the chip package. The crossing of pins 7 and 8 of U2' is permitted because the wire-bonding machine employs the use of insulated bonding wires to prevent short circuits within the chip package. The packaged (assembled) U2' is delivered to the board assembler who uses standard SMT assembly practices to mount U2' along with the other components on the Bill of Materials (BOM) to complete the board assembly. Though the above examples in Figure 3 and Figure 4 are simplistic, the same process is applied to complex board designs.

The board has the opportunity for improved circuit speed roughly equal to one nanosecond (in a theoretical lossless substrate) for each 6-inch (150mm) reduction of dual copper path (signal plus ground) according to the speed of light formula.

The same standard JEDEC IC packages such as QFN, QFP, SOIC, BGA, CSP, TSOP are used in Chip Packaging 2.0 just as in Chip Packaging 1.0. A hallmark of Chip Packaging 1.0 is that wire bonding inside the IC package from silicon die to the lead-frame (or substrate) is neat and orderly. However, Chip Packaging 2.0 permits the silicon to be wire bonded with insulated wires (a bond wire innovation from Microbonds) that crisscross in a "bird's nest" manner across the die in every direction. In the Chip Packaging 2.0 environment, "neat and orderly" is replaced with "disorderly esthetics". But the result is truly optimized wires that cross over one other as shown in Figure 5 and 6.
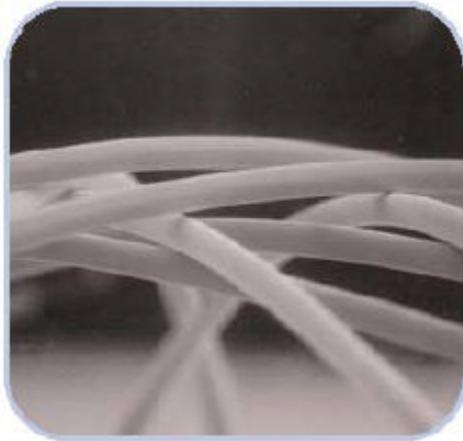

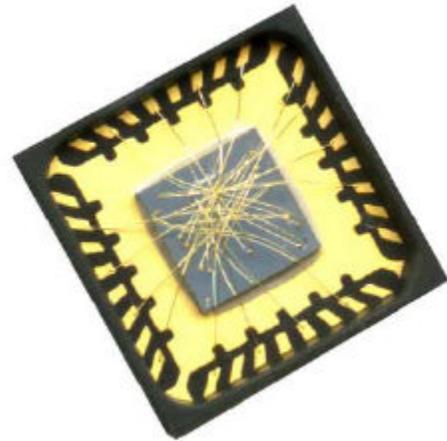Figure 5. Insulated bonding wires safely allow wires to cross.

Figure 6. Example of open cavity QFN with crossing insulated bonding wires.

The cumulative sum total thickness of crossing bonding wires cannot exceed the maximum "headroom" of the IC package. About 15-mils of "headroom" is normally required between the upper most wire and the internal ceiling of the plastic IC package. Assuming that typical insulated bonding wire is 1-mil in diameter, the maximum number of crossing wires is easily calculable, after taking into consideration the thickness of the die and thickness of the lead frame. The EDA software calculates the maximum number of wires that are allowed to cross. Other issues involving grounding, shielding, cross talk and EMI need to be meted out and resolved.

In the ramp up of production, once non-recurring costs of Chip Packaging 2.0 are cycled out, it is anticipated that the total cost of ownership of these systems will be lower due to the decreased usage of raw material (smaller boards with fewer inner layers supporting smaller cabinetry resulting in reduced cost) and the benefited economic value of bringing boards to market quicker than competitors. Since Chip Packaging 2.0 board designs have the potential of being simpler, it is anticipated that there will be a lowering of costs related to testing, rework and field failures.

There will likely be issues to be resolved along the way to making Chip Packaging 2.0 a standard industry practice. EDA optimization software must be developed and be economically available for mainstream board designers to use, but there appear to be no major roadblocks. Several EDA software companies are moving along in that direction.

Anyone who has purchased traditional Chip Packaging 1.0 design software knows how the sticker shock associated with such software products. A low cost solution in the Chip Packaging 2.0 environment might be to allow board designers nearly free use of EDA chip iteration software during the optimization period, and then charge a reasonable license fee based on a "pay per use" basis. In such way, under budgeted design departments can have free access to the necessary EDA software during the design period, and once the board is optimized, and ready for fabrication, that's when the software company gets compensated. Customers would love that.

In summary, a means for empowering board designers to optimize board-level designs by re-mapping pinouts of legacy die in a proposed Chip Packaging 2.0 world has been described. It was noted that in the current Chip Packaging 1.0 environment, there is little interest by legacy chip designers to collaborate with board designers. Aside from what is written in a manufacturer's data sheet, there is limited communication channel for board designers to discuss modification of legacy die package pinouts. Further, it has been observed that packaged chips are routinely thrown "over the wall" for board designers to deal with.

In Chip Packaging 2.0 we ask the question *"what if"* board designers were empowered to re-map legacy package pinouts (without changing the performance of the silicon) in order to design optimum PC boards? To usher in the new era of Chip Packaging 2.0, it is necessary that suitable EDA software be readily and economically available to board designers to re-map legacy chip pinouts while simultaneously optimizing the board. The appropriate software creates the requisite chip pinout-bonding schedule and seamlessly delivers it to wire bonding machines via the Internet (or by conventional means) to assemble "User Definable Pinout" (UDPo) packages according to the customer's (board designer's) requirements. We hope that this article stimulates thinking relative to the topic of Chip Packaging 2.0 and encourages interested parties to actively engage in discussion.

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