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Wafer-Level Die Stacking and Assembly

ET-Trends LLC has filed patents dealing with wafer-level die stacking. Today, the "pyramid" die stacking process involves assembling individual die, one on top of another, until the desired number of chips is configured. This new method could streamline the 3D die stacking process in two fundamental ways. First, the back of the wafer can be coated with high-performance thermoplastic die attach adhesive. The liquid adhesive, that may be electrically and thermally conductive, is applied to the wafer by stencil printing or other means. The coating is then hardened to a tack free film that permits the wafer to be handled and shipped. A direct film bonding process can also be used. A wide range of adhesives are available with various fillers and bonding temperatures. B-staged thermoset adhesives can also be used.

The adhesive-coated wafer is next singulated by traditional sawing methods. The high-molecular weight thermoplastic adhesives do not interfere with sawing provided that the cutting zone temperature does not exceed the softening point of the adhesive that can be greater than 300^{o}C. Good results have been obtained with standard equipment.

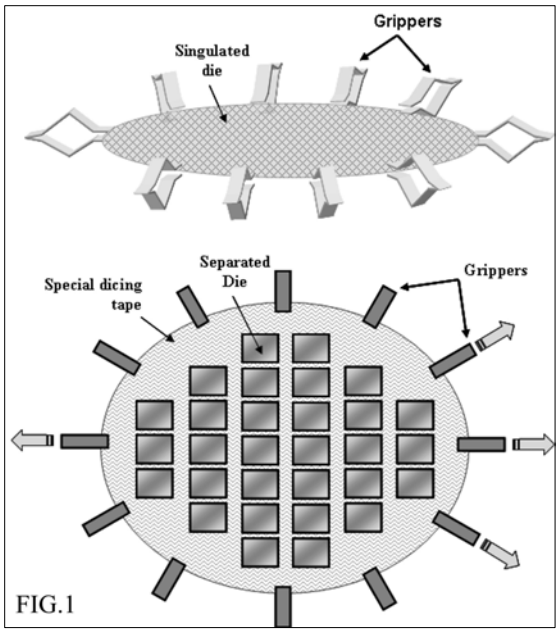


FIG.1

The sawn wafer is now ready for expansion. The dicing tape is actually a high-elongation elastomer that may have a dot-like pattern of adhesive instead of the normal continuous coating. The tape is next stretched, or expanded, using edge grippers, or other means, to pull outwardly until the desired die spacing is achieved as shown in Figure 1. The expanded wafer is then aligned with a second wafer that may comprise larger die. The second, or bottom wafer, is bonded to the top wafer by applying heat and pressure. The heat-activated adhesives can provide a strong bond that meet MIL STD 883 criteria. The tape is then removed leaving a 2-level die stack. UV-release adhesives are well suited for the application to reduce mechanical stress and contamination. The steps can be repeated using wafers with progressively smaller die until the die pyramid is complete. The bottom, or base wafer, can be sawn at the packaging stage unless diced earlier.

The process can deliver die stacks efficiently assembled and tested at wafer-level. The use of a thermoplastic die attach adhesive allows wafer-level coating while also providing advantages over traditional thermoset pastes. There is almost no adhesive squeeze-out, adhesive thickness is very precise, die stack planarity is assured, adhesive ionic content is essential zero, and adhesive properties are extremely stable. Thermoplastic die attach adhesives are typically shipped and stored at room temperature, unlike thermosets that require freezer conditions. Since thermoplastics are reworkable, a die can be removed or repositioned if required. Thermoplastic adhesives are available with a wide range of modulus values and these materials are recognized for their low outgassing. However, the wafer stacking process can also be used with standard thermoset die attach pastes or B-staged products. Thermoset pastes can be applied to wafers by needle dispensing, stencil printing or jetting providing significant efficiencies and lower costs. Figure 2 shows the wafer-bonding step that can be repeated for higher stacks.

The process can also be used to assemble flip chips to die with backside bond pads or to chip carriers provided that the spacing requirements do not exceed the tape expansion limits. Note that the tape expansion does not need to be symmetrical; X and Y extension can be different as seen in Figure 1. Asymmetrical expansion can be used for precision wafer alignment or to accommodate chips that are rectangular.

In the future, a bumped wafer might be coated with wafer-level underfill (WUF), the tape then expanded, and the chips bonded to packaging substrate. This approach would be especially suitable for CSP carriers that would not require excessive expansion. The process is being considered for massively parallel RFID tag assembly but larger antennas may be outside of the tape expansion limits. Figure 2 shows the wafer-level bonding processes using wafer-coated die attach adhesive to produce a 2-die stack (shown for simplicity). Process repetition would produce higher stacks. Mixed stacks of wire bond die and flip chips would also be possible.

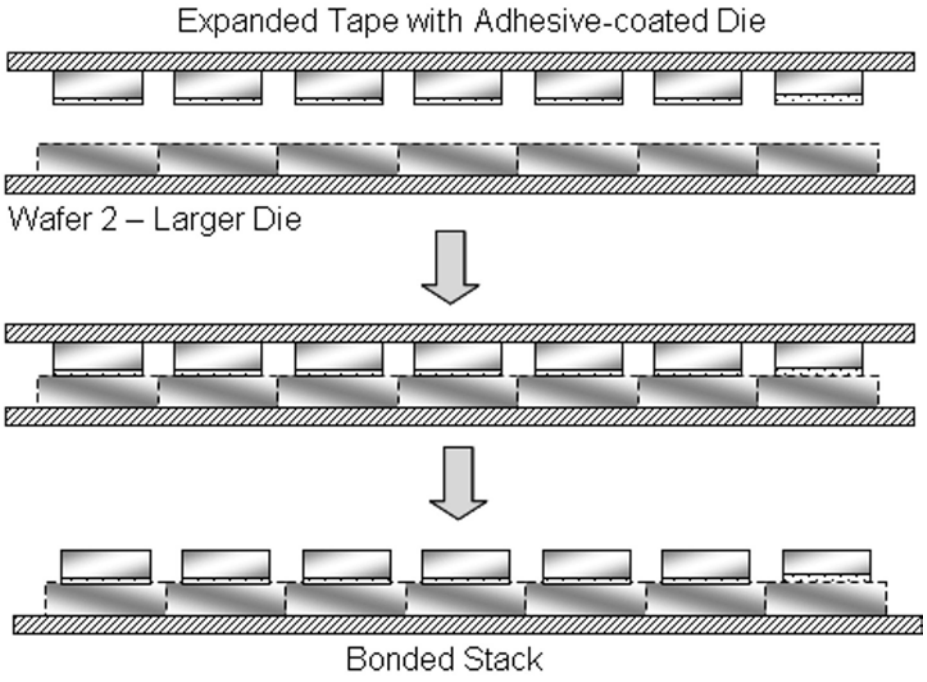
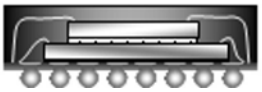


FIG.2



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