Onward and Upward - from Pyramids to Blocks

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Semiconductor memory modules and other solid-state products, especially sensors, have used 3D chip stacking for more than a decade. A few optical products used piggybacked chips over 20-years ago (e.g.; Motorola Optobus). Although *"flip chip on chip"* has been used, one of the simplest and popular schemes is to stack decreasingly smaller chips on top of one another to form a "pyramid" (aka "wedding cake"). The pyramid design permits the use of mostly standard processes with existing equipment. Ubiquitous wire bonding can be used with only minor changes although wire bonders are now available that are specialized for multi-plane applications. Staying within the boundaries of the infrastructure is the first choice for manufacturing and generally works for technology evolutions. But pyramid 3D stacking is about to get some serious competition from the semiconductor industry and it could be disruptive.

The packaging industry has undergone at least three major transitions in its century of progress that began with glass hermetic packaging in the form of cathode ray tubes (1897) and radio vacuum tubes (early 1900's). About 50-years later, successful implementation of ***plastic non-hermetic packaging*** heralded a major breakthrough - a bona fide revolution that helped reduce cost and enable automation. Later SMT, and then Area Array, were major events. Some have suggested that multichip packaging was the 4th major event, but "multichip" (multi-component) modules were produced even before the transistor. Others may offer that Chip Scale Package (CPS) was a breakthrough, but even smaller, chip-size flip chip and short-lead direct mount packages were known by the 1960's. What about wafer-level packaging (WLP) and 3D stacking? What if we combine them! Is this worthy of the "technical revolution" moniker?

A number of researchers in the semiconductor field have been working on through-vias, often called ***through-silicon vias*** (TSV). While the concept is simple, the necessary processes represent a very significant challenge. Considerable difficulty results from having to handle delicate wafers, often thinned, and creating conductive vias that are in the nanoscale range. First, tiny vias must be formed through the wafers using chemical etching, laser drilling, or one of several "energy" methods, such as RIE (Reactive Ion Etching). MEMS (Micro-Electro-Mechanical Systems) has long used selective silicon removal processes to produce 3D chip structures and some of these methods have been adopted for TSV. But the vast array of vias must be accurately located and have an acceptable cross-sectional profile. Once the through-vias have been properly fabricated, they must be made electrically conductive. Finally, the wafer stack must be precisely aligned and bonded. This task set has many parallels to building multilayer PCBs. In fact, copper plating is a popular TSV method, although vias can also be filled with conductive materials. There are already around 500 US patents and applications covering TSVs, and many deal with copper plating that isn't much different from modern PCB micro-via methods.

The wafer-bonding step has many options that were mostly developed by the MEMS community. But there is no clear winner yet. Some favor use of a bonding interface material, such as an interposer film, while others use one of several direct wafer-to-wafer bonding methods. The wafers can also be bumped and then joined. A few patents even describe carbon nanotubes (CNT) for through-via conductors/connectors. Once the stack is bonded, a base must be added or formed to enable assembly to a PCB. The simplest approach is to add solder bumps to create a BGA, or 3D flip chip. The final step is wafer singulation.

Will TSV become a success and when? Yes, and sooner than you might expect! During the writing of this article, IBM announced a 3-D chip TSV breakthrough chip-stacking technology and noted that it was the result of more than a decade of research. According to their press releases (www.ibm.com), IBM is already running TSV in a manufacturing line and will begin sampling TSV chip stacks in Q2-2008. IBM claims that TSV shortens the distance that on-chip data must travel by 1000 times and allows for the addition of up to 100 times more channels; equates to a major performance boost. But it also reduces the package footprint more than any other technology. While major memory makers see TSV as perfect for their products, IBM will apply the stacking to just about everything, from telecom to mainframe CPUs. TSV just may be the *final packaging revolution* and it will have a major impact on packaging logistics. The fabs will almost certainly do the TSV process, but some foundries may sell a complete assembly-ready package.

Since there's a long list of TSV developers, including Elpida, Fujitsu, IBM, Intel, Micron, Samsung, Rambus, Toshiba and many others, this is a race worth watching.

Here's a final thought on multilayer. TSV 3D may be the ultimate package (until we enter the post-silicon era), but it took quite a long time. Hold it! Isn't "multilayer" just an old idea that we in the printed circuit industry invented a 100 years ago? But, of course, and we did it from the beginning with copper. The semiconductor guys switched from aluminum conductors to copper just over a decade ago. And while the semiconductor dudes are just learning how to build multilayer wafers, our multilayer circuit board idea has been around since 1902. And it's about time that the semiconductor industry started trying out our tried and true methods, even if they think they're at the *top of the pyramid*.

FIGURE: Left shows first PCBs multilayer patent; right shows a TSV sample from Samsung.