Wafer-Level Flux-Underfill: *Underflip*!

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Introduction

As the saying goes, there's more than one way to skin a cat and there's also more than one way to underfill a package. First, let's define underfill in terms of function before dealing with application methods. Underfill is a specialized laminating adhesive that mechanically couples the bottom surface of a chip or package to the top surface of the substrate. The main purpose is to mechanically lock the two dissimilar structures together thus reducing or even eliminating the differential movement in the X-Y plane that would occur during thermal cycling. A strain relief mechanism must be provided to deal with potentially catastrophic strain produced during thermal excursions whenever such dissimilar materials are joined.

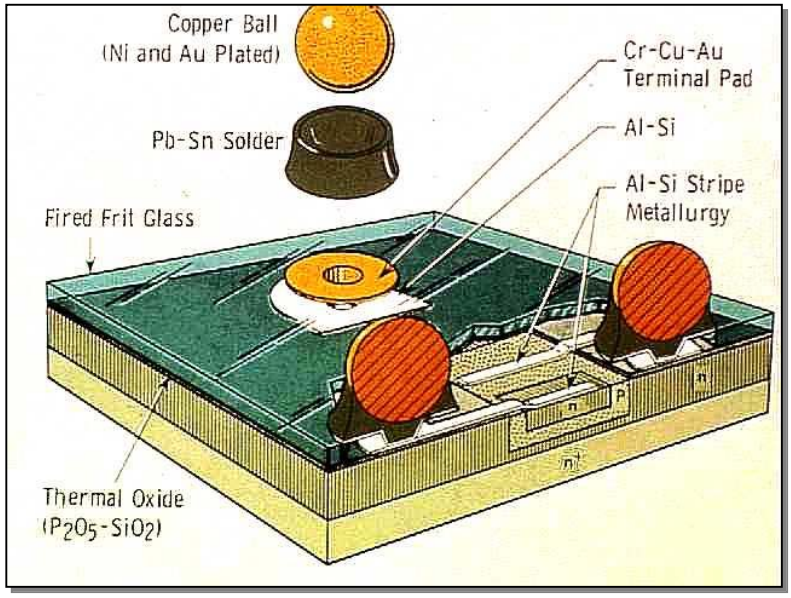
The underfill adhesive simply bonds the low-expansion, high-modulus chip to the higher-expansion, lower-modulus substrate that is typically used with Flip Chip on organic. The very stiff silicon chip constrains the X-Y movement of the substrate so that it is forced to mimic the thermomechanical behavior of the chip. The net result is that the two interfaces expand and contract in harmony to reduce strain on any vertical interconnecting structure such as bumps. Please note that underfill transfers the low expansion property of the chip to the substrate. The Coefficient of Thermal Expansion (CTE) of the underfill is of secondary importance within the X-Y plane.

The situation in the Z-direction is entirely different and is somewhat independent of X-Y movement if we exclude warpage effects. The only constraining force in the vertical direction from the package is the relatively small one due to the bumps. Since the underfill area typically occupies a much greater percentage than the bumps, its thermomechanical properties will determine Z-direction expansion rate. This is the principal reason why the CTE of underfill should approximate that of the bumps or other interconnect structure. High expansion underfill will "stretch" the bumps during heating and compress them on cooling to eventually cause fatigue fracturing. This is why most underfills contain silica filler. Now let's review Flip Chip.

DCA Technology

At the beginning of solid state electronic packaging, there were only two primary chip-level interconnects – *wires and joints*. Three decades later, there are still only two; *wires and joints*. TAB (Tape Automated Bonding), a beam lead interconnect system, is still wire albeit chemically crafted wire. IBM was the first to commercialize chip-level **joint** connections with SLT (Solid Logic Technology), a transistor package using solid copper balls (the first BGA) to fabricate the first high volume Flip Chip. This was even before the famous C4 product with solder bumps. IBM's Paul Totta, *Emeritus Fellow*, points out that the Flip Chip work

really began about 40 years ago (1961). The historic but remarkably modern SLT is shown in Figure 1.



[Figure 1 – SLT courtesy of IBM**]**

During the 1960's, IBM, Delco and others launched Flip Chip into high volume, highly successful production. But the FC was only implemented on ceramic substrates. Back then, ceramics were the premiere high density, high reliability printed circuits. These ceramics provided the high density for mainframes, the durability and robustness for under-hood automotive but also the *close-enough* thermomechanical match for low strain Flip Chip assembly. Special ceramic materials were even developed with CTEs that came close to matching the chip. First generation FC solved problems by tailoring the substrate.

Cost Reduction and 2nd Generation Flip Chip

Most recently, Flip Chip has experienced a reawakening with the support of new technology for its transition. Motorola and other vertically integrated electronics companies began to move Flip Chip into the consumer product area where lower cost substrate was required. Some of us have referred to the 1990's shift to organic substrate as 2nd generation FC. The substrate substitution has had major ramifications, however. The inherent high reliability of the silicon-on-ceramic system was not to be achieved with silicon-on-organic structures without additional technology. The near-match for CTEs for the early systems gave sufficient reliability, especially with the smaller FCs then in use. But the order-of-magnitude mismatch for organics devastated reliability during thermocycling. The seemingly simplest solution was to add underfill between chip and substrate.

The 2nd generation FC would seem to be all we could want in a package – density, high speed, and lower cost; the epitome of *smaller-faster-cheaper*. Yet

there are at least two notable problems. One is die shrink, the size reduction of the IC geometry, frequently used to increase performance and productivity (more chips per wafer) while cutting cost. The die shrink downside is that the chip gets outwardly smaller and that's good in most situations. But if the chip pad footprint changes, this is a problem for Direct Attach Connections. While wire bonders only need re-program, FC assemblers may need a new circuit board. The CSP community may also need to re-fabricate their packages, but that's easier than modifying an entire multilayer PCB. There may not be an easy solution here. Bumps can be rerouted or the initial bump pattern can be pre-shrunk so that the same layout works for the 1st and maybe the 2nd shrink. Sooner or later the FC doesn't fit the circuit PCB pads.

However, there is a more critical problem affecting most FCs – UNDERFILL! Not the material, but the process. Polymerized underfill works reasonably well and adds only a miniscule amount of material cost. But the common capillary flow-underfilling step wreaks havoc with the SMT methodology. Flip Chip starts off as a clean and simple SMT process with the assembly solder built right into the chip for eutectic bumped chips. The self-alignment performance of FC is extraordinary as has been shown in videos. But just when the process should be complete, another non-standard step is starting – underfilling. It's not the fill - it's the filling that hurts!

So with the successful implementation of 2nd generation Flip Chip brought about by the underfill solution, we would like to say, "And the rest is history", but cannot. Unfortunately, the solution is becoming a more significant problem as FC assemblers become more advanced. The advent of high volume Flip Chip has focused more and more attention onto manufacturing issues. So while underfill, provided reliability, it added an "alien" process that is a poor fit with in-line SMT assembly. *Underfill was the solution yesterday, but it's the problem today*.

The Productivity Issue

Many of us thought that the new *snap flow snap cure* underfills [1] would alleviate the manufacturing issues. Better capillary flow underfills would break the *bottleneck* so enthusiastically spotlighted by the CSP leaders. But did the "snappy" underfills break bottlenecks and set records? As it turns out, the fast flowing 5-minute cure state-of-the-art capillary flow underfills still aren't quick enough to wring out cost and aggravation for many products. And these newer materials have reached a performance plateau and may be close to the ***laws-of-science*** barriers. Yes, the capillary flow products work and they're in production throughout the world, but industry demands real productivity, much more productivity and fewer steps.

Underfilling can be the *epitome of exasperation* from the assembler's point of view. The underfilling process is more than a nuisance, it adds a significant amount of cost when we rigorously analyze productivity. Even a few seconds of

added cycle time will translate into a large sum of money at the end of the day - a fortune at the end of the year. The cycle time increase will typically add more cost than the small savings that “no package” can offset. Once again, the underfill material cost is not the core problem – it’s rather insignificant. But the underfilling step can increase manufacturing time by 50%, double floor space requirements and add significant dollars in capital equipment. We have estimated that reduced productivity from underfilling may add an extra 1-2 billion dollars per year in reduced output [2]. But do we really know how best to apply underfill?

Basic Classes of Underfill

Once applied and cured, underfills end up being hard solids with good adhesive properties and are really quite similar. It is the method and point of application that really determines the class of the underfill. Table 1 categorizes underfill on the basis of physical state and point of application in the process. The table includes solid underfills and this should not come as a surprise that they can start off as solids. We use a variety of solids in electronics, including solders that are momentarily in a liquid state only during processing.

The first demarcation, however, is determined by *point of applied* in the process - before or after assembly to substrate. We are most familiar with *de facto* standard type underfills that are post-dispensed and commonly called capillary flow underfill. But this class is the slowest to process for several reasons and the one giving underfill a bad rap. First, the capillary flow process involves the most steps: (1) flux site, (2) place chip, (3) reflow, (4) underfill and (5) seal or fillet. The new pre-dispensed underfill classes offer productivity by combining steps.

Table 1

1.0 **Post-Dispensed *Liquid*** *– capillary flow – the standard today*
2.0 Post-Dispensed ***Solid*** as received, molded underfill; MUF
3.0 **Pre-Dispense**
3.1 On Substrate
3.1.1 Liquid; “No Flow” 3.1.2 Solid (Film)
3.2 On Chip/Wafer
3.2.1 Liquid (not practical) 3.2.2 Solid Wafer Level (W-L)

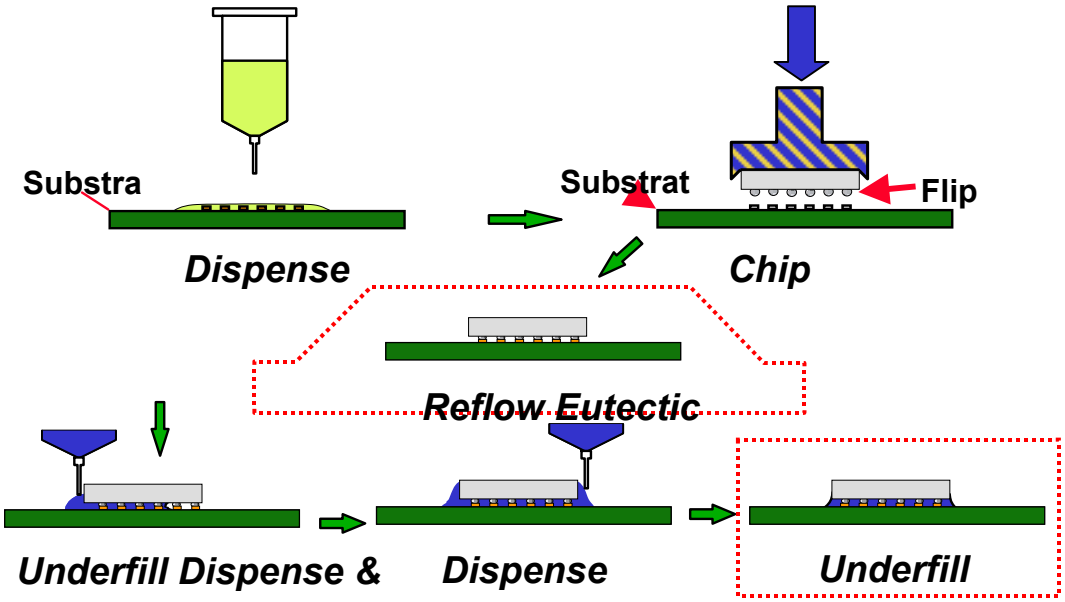
New Molded Underfill Process (MUF)

Before moving to pre-dispensed underfill, it is worth noting progress in the exciting under-molding process area. Transfer molding has been the workhorse method for encapsulating packages for decades. The molding process has been successfully ported to area array packages like BGAs and CSPs with the

development of low warp epoxy molding compounds (EMC). During 1999, new mold designs and materials made it possible to mold underfill. The MUF process seems especially valuable for Flip Chip in Package (FCIP) where high volume is common. The MUF process can also permit simultaneous overmolding to produce a fully protected package. We hope to report more at a later date. Now lets move on to pre-dispensed materials.

Pre-Dispensed Underfills

Several companies and universities pursued this pre-dispensed underfill area of development beginning in the early 1990's. Many problems were encountered for the pre-applied flux-underfills, but thanks to a long and intensive effort, especially by Professor Dan Baldwin, his students and associates at Georgia Tech, a practical process has been developed and reliability data is available. Several companies have or will soon introduce pre-applied flux-underfill products although the technology has not yet gained wide acceptance.
The pre-applied flux-underfills are also called fluxfills, "no flows" and other obvious names that will likely become trademarks. This initial class of the pre-dispensed variety does have limitations that can make them unsuitable for some FC assemblies. The first issue is that today's products are unfilled systems. The addition of inorganic fillers, like silica, interferes with soldering to significantly reduce yield. Lack of filler results in a higher CTE (Coefficient of Thermal Expansion) compared to capillary flow products. The optimum CTE value is a match to the solder joint - 25 ppm/^{o}C. The "no filler" products have values as high as 75 ppm/^{o}C creating more stress. Still, some of these materials have passed 1000 cycles @ -55^{o}C to 125^{o}C with smaller (0.250" die) [3]. Although the pre-dispensed liquids are not perfect, they bring us much closer to running Flip Chip as a standard SMT process.



[Figure 2 –No Flow Process]

What's Next for Underfills

So how can we take the next step along the road to success in making Flip Chip the ultimate package? Wafer-Level processing offers a high leverage and productivity for many semiconductor products and some packages. This generally requires solid materials if the singulated chip is to be easily handled and transported. This would also require a system that could be momentarily melted or softened and then hardened again. But is such a system feasible? We can find the answer by looking at the other side of the chip or wafer – die attach!

Solid die attach films, such as Staystik®, have been used to bond large and small die for the past decade. They employ thermoplastic polymers that can be coated, cast, printed and stenciled. The solid thermoplastics can be softened by heating to allow bonding to occur and then cooled to yield a stable assembly. These low stress thermoplastics have established an excellent record as die attach products. Why not use the thermoplastic concept for the flip side of the chip? How would the thermoplastic solid underfill be applied?

Significantly, one die attach adhesive application process involves wafer-level (W-L) coating. The thermoplastic is made into a coatable solution and then stenciled, sprayed or spin-coated onto the wafer. Baking hardens the material and the coated wafer is finally sawn. The resulting ***ready-to-bond*** chips can be easily handled and quickly bonded by heat activation. There is no curing, no chemical processing and no surprises - only the simple physics of melting, bonding and cooling the pre-polymerized adhesive. One added benefit is long shelf life with room temperature storage. Another benefit is reworkability. Unlike thermosets, the thermoplastic adhesives are reworkable.

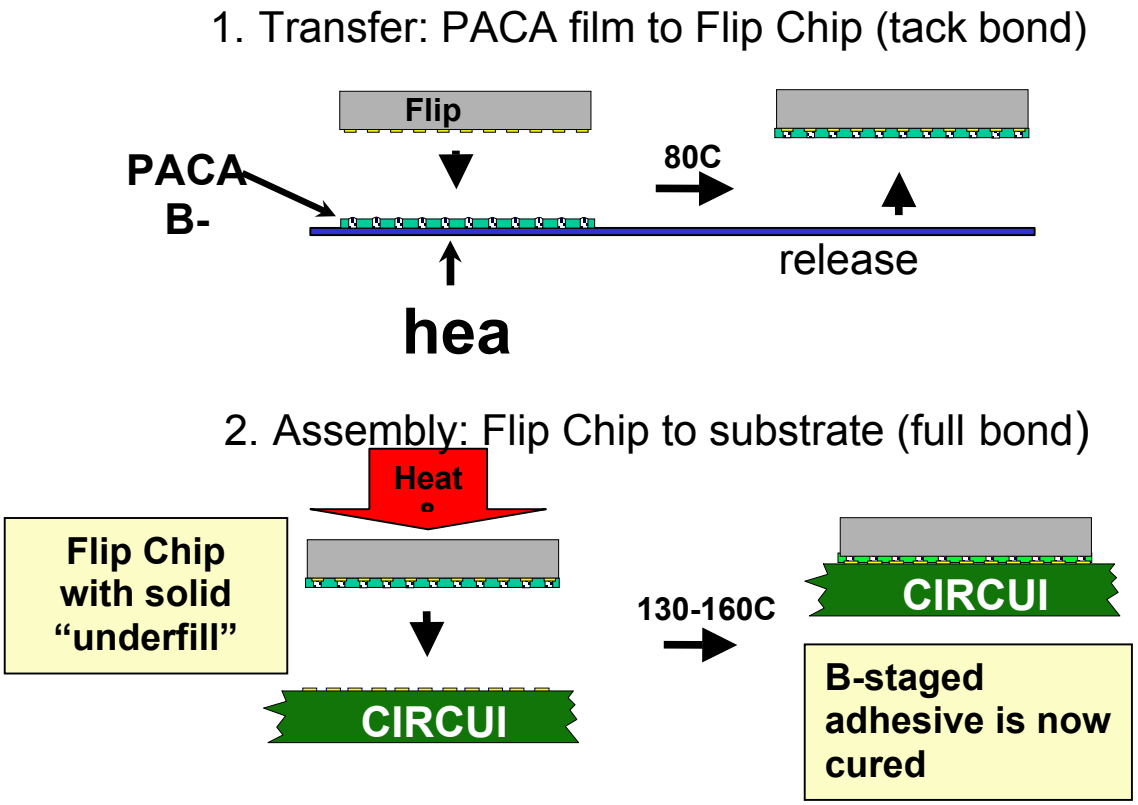
How can this technology be applied to underfill? Recall that the primary purpose of underfill is to strongly bond the chip to substrate. This is also the main purpose of the die attach adhesive. In other words, underfill and die attach adhesives have a lot in common. Underfill adhesives, of course, must always be a good electrical insulator while die attach adhesives are often conductive, but this is simply a matter of filler choice. The main processing difference is that underfill would need to be coated onto the face of the wafer with bumps present (but not in all strategies). Certainly this is more challenging than coating the smooth backside of a wafer, but it is feasible. Stencil printing rather than spin coating could be used to avoid "shadowing".

Solid Underfill in Use Today?

Many observant technologists have remarked that anisotropic conductive adhesives (ACA) eliminate the underfill. Actually, the ACA embodies a built-in underfill. The dielectric adhesive part of the ACA is essentially an underfill. There are actually two classes of anisotropic adhesives; those with randomly dispersed conductive particles, called random anisotropic conductive adhesives (RACA)

and a patterned array type. The second less common type, the patterned anisotropic conductive adhesive (PACA), is really a composite of underfill adhesive with an array of conductive adhesive "islands". In fact, materials have been developed using B-staged silica-filled epoxies as the dielectric. Some of these PACAs have been designed for Flip Chip [4]. Figure 3 shows a PACA process.

[Figure 3 – PACA Process]



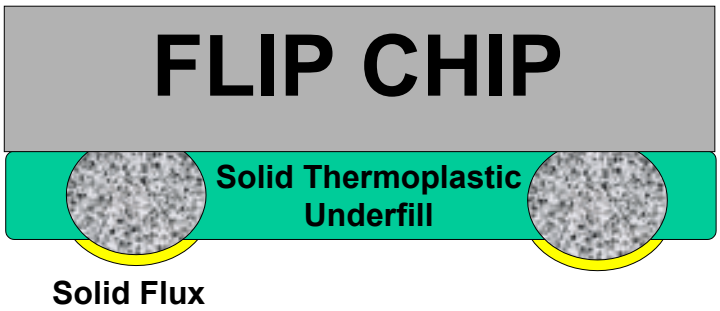
Flipped Underfill = "UnderFlip"

Now we will focus on solid underfill. We now report work on solid flux and underfill that is specifically intended for wafer-level application to Flip Chip and other array products. Table 2 outlines possible strategies and all have been investigated. Most of the work has focused on thermoplastics since these materials could also impart reworkability just like the case with die attach adhesives. Thermoplastics, unlike thermosets, can be repeatedly melted and hardened just like solder. Thermoplastics are the organic analogs of solder and have been called "polymer solders" or "organic solders" [5]. Note that pre-polymerized thermoplastics have not been used for capillary flow underfill because they are made into liquids by adding solvent. Solvent evaporation within the confines of an assembled Flip Chip would produce unacceptable voids and shrinkage upon drying.

Table 2

1. **Two-Layer System** – separate flux and underfill
2. **Single Thermoplastic Layer** - with fluxing properties
3. **Single B-Staged Thermoset** - with initial flux properties
4. **Material Applied to Unbumped Wafer** - used also as a bumping mask

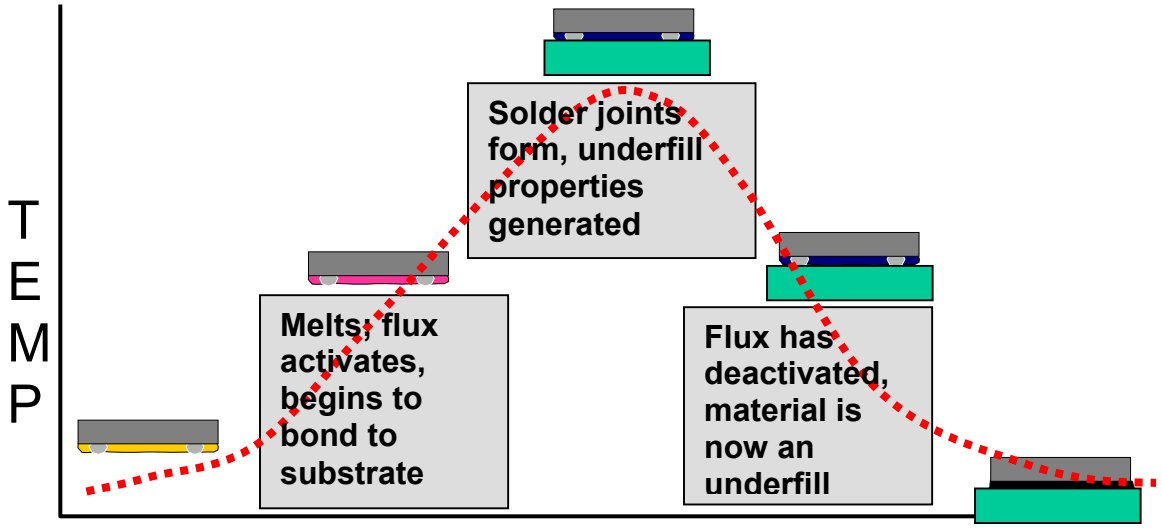
The W-L flux- and underfill-coated Flip Chip can be a true SMT package, but assembly must occur without the use of external force to the chip. Concept testing has led us to maintain separate underfill and flux layers although a single flux-underfill material could be useful. There are two reasons for the two-layer approach. First, it is easier to optimize the individual sets of flux and underfill properties without compromise. Secondly, the underfill, or "underflip" layer, may contain filler since this will not interfere with soldering as is the case with liquid "no flows" flux-underfill. The flux layer should not contain filler since this is the material that will cover the bump or even surround it. Figure 4 shows the two-layer concept but there are many possibilities including bumps that are fully surrounded by the flux [6, 7].



[Figure 4 – W-L FC]

Our preferred solid flux is a modification of the liquid ChipFlux 2020 epoxy-based system that has been in commercial use for many years for use as a no clean underfill-compatible flux for FCs. The first task was to select solid epoxy resins and choose appropriate solvents. The balanced selection of solid epoxy, flux-active hardener, solvent and tackifier allows the formulation of coatable flux with an engineered melting ranging from 60°C up to 160°C. The level of tackiness needed for holding the chip in place prior to reflow can be adjusted. The solid version of ChipFlux 2020 is providing good soldering and joint formation in FC assembly testing. The flux is thermally-converted to a strongly bonding inert polymer that can also serve as a primer for the thermoplastic underfill layer that does not really need to melt during reflow. The use of flux-active hardeners for epoxies is protected by U.S. patent 5,904,782 [8]**.** Figure 5 depicts the proposed FC=SMT® process.

[Figure 5 – Reflow Profile from ppt.]



Application Methods

There are several practical wafer-coating methods. Stenciling, one of the successful processes used for die attach pastes, can also be used here without damaging bumps. Work at Speedline/MPM and Georgia Tech are still defining the parameters. Spin coating, as might be expected, can cause shadowing by the bumps as a material is spun out from the center. It still may be possible to use spin coating followed by a leveling step. Spraying and curtain coating are other possibilities. Some variations of the process involve coating the bumps with flux prior to underfill application. Once coated, the underfill layer is dried to a solid film in an oven. Methods have been worked out for sawing the wafer.

Flux paste can be selectively applied to bumps by roller coating or wafer dipping. The wafer dipping approach is similar to the flux application process for single Flip Chips using a rotating drum. The required amount of paste is spread out on a very smooth and planar rotating disk using a precision doctor blade. The solder-bumped chip or wafer is pressed into this reservoir with bumps down and then withdrawn. Bumps become coated with a specific amount of material that is determined by doctor blade height, withdrawal rate, bump geometry and the paste rheology. The right flux, however, can be coated onto the thermoplastic layer to produce a continuous film. This approach lets the flux also act as a primer. Keeping the flux layer thin eliminates the need for filler that could interfere with joint formation.

Future Work

During the remainder of 2000, work will continue on W-L application methods and SMT Flip Chip assembly at Cookson, Alpha Metals, SCS, Georgia Tech and Binghamton University with materials modification as required. Beta site testing is

expected in mid-2000 and positive results could lead to a product introduction in the same year.

Success with this Ready-to-Bond FC concept or any other that enables FC=SMT® should radically enhance the value of Flip Chip. The underfill process will become transparent to the assembler. There will be no extra-step penalties for assembly and the FC will be just another SMD. Triumph over today's underfill limitations will take Flip Chip to the next and final level - a true package [9].

The result: **FC=CSP**.

Reference

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[9] Gilleo, K., "Chip Scale or Flip Scale: The Wrong Question?", pp. 30, 31 - 34, Circuits Assembly, Feb. 1998.

Trademarks

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